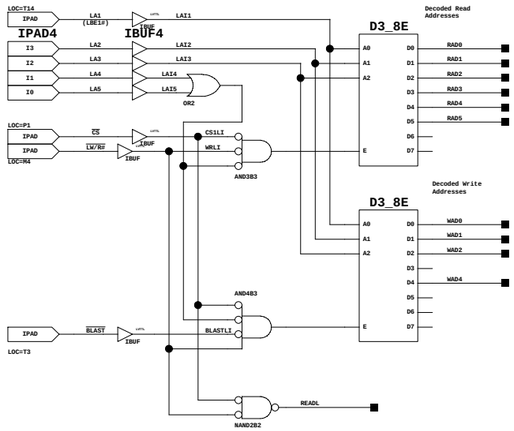
FILE: IBAFPGA	DWG:

REV.	APPROVED	DATE



MARK 5A INPUT FPGA CONTROL BITS									
		15	12	11	8	7	4	3	0
ADDR	TYPE								
0	Read/Write				R	U	Clock Generator Frequency		
1	Read/Write					V	MODE		
2									W
3	Read Only								E
4	Read/Write						RECORD Clock OFF		F
5	Read Only						Design Version Number		

V => VLBA Mode (Ignored)

W => Clock Generator Word Load Clock (W_CLK)

U => Update Frequency (FQ_UD)

R => Reset (Initialize) Clock Generator

E => Odd Rack ID Error

F => RECORD Clock OFF

MODE

0100 Straight Through Mark 5P Compatibility Mode

0000 32 Track Mode

0001 64 Track Mode Multiplexed 64:32

0010 16 Track Mode De-Multiplexed 16:32

0011 8 Track Mode De-Multiplexed 8:32

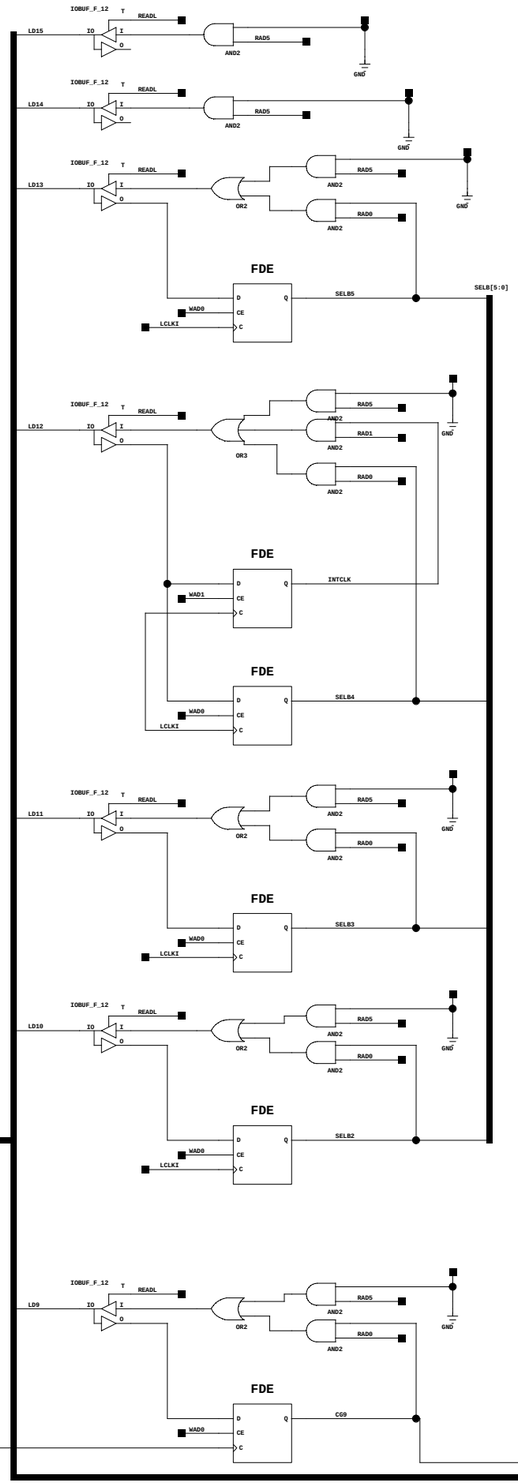
1000 Test Vector Generator Mode

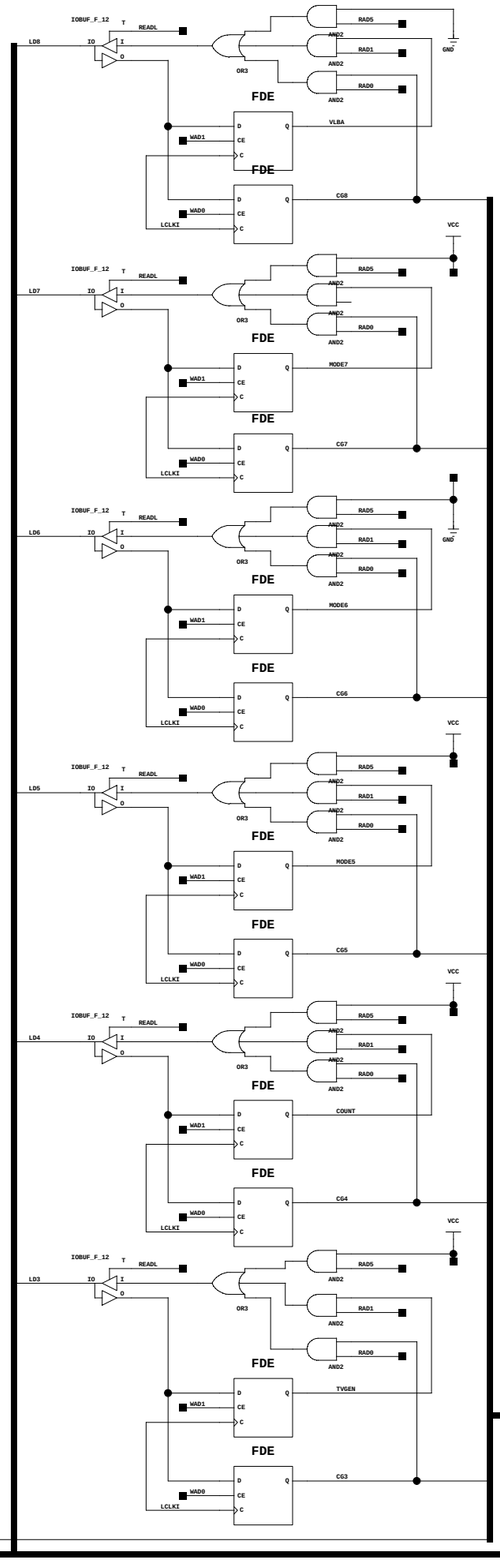
IOPAD16

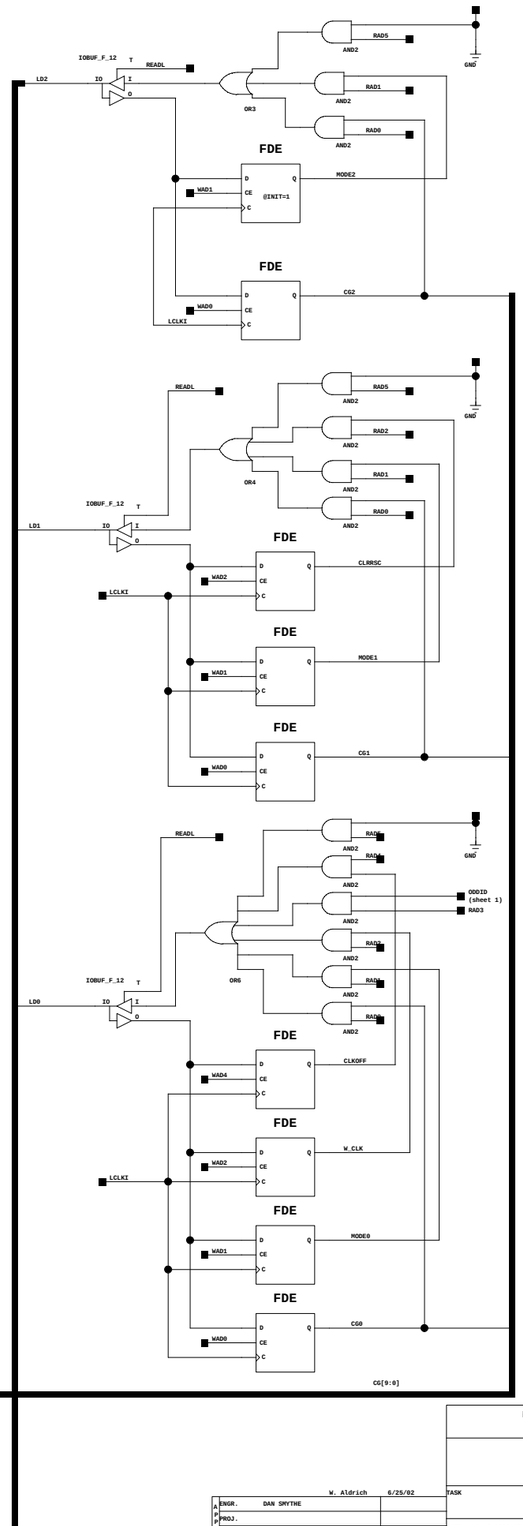
IO[15:0]

LD[15:0]

LCLKI







NEROC - HAYSTACK OBSERVATORY WESTFORD, MA 01886			
MARK 5A INPUT FPGA PCI INTERFACE			
	W. Aldrich 6/25/02	TASK	SIZE D / DWG. NO. / REV.
APPROVED ENGR. DAN SMYTHE			
PROJ.		DATE 6-18-2003_13:49	SHEET 4 OF 4
PROG.			