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19 April 2007
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Subject: **MARK5B DOM SOFTWARE REGISTER MAP** Rev 1.8

Note: Addresses used in this document are an offset, relative to the base address of the DOM. The '_' character in the addresses is purely for readability.Bit fields marked as unimplemented will read back undefined values and cannot be successfully written. Unless otherwise noted the reset value of all bits is '0'. In all cases, mode codes which are undefined should not be used.

GLOBAL REGISTERS

0x00_0000	Enables Register
0x00_0001	Status Register
0x00_0002	ICLK Control
0x00_0003	DOM Resets0
0x00_0004	DOM Resets1
0x00_0005	SDRAM Address0
0x00_0006	SDRAM Address1
0x00_0007	DOM Known Register
0x00_0008	DOM Scratch Register
0x00_0009	DOM Control Register
0x00_000A	DOM Interrupt Mask Register
0x00_000B	DOM Interrupt Register
0x00_000C	DOM Correlator Frame Interrupt Counter

STRIP HEADER MODULE

0x00_1000	StreamStor Invalid Reg0
0x00_1001	StreamStor Invalid Reg1
0x00_1002	DIM Invalid Reg0
0x00_1003	DIM Invalid Reg1
0x00_1004	Disk Frames per Second
0x00_1005	Disk Frame VLBA Time Code0
0x00_1006	Disk Frame VLBA Time Code1
0x00_1007	TOT Count

UNPACK XBAR REGISTERS

0x00_2000 – 0x00_201F	Xbar Slice Setting RegN
0x00_2020	Unpack Code

CORRELATOR FRAME HEADER RAM BANK

0x00_3000 – 0x00_30EF	Correlator Frame Header RAM Bank A
0x00_3100 – 0x00_31EF	Correlator Frame Header RAM Bank B

DELAY GENERATOR

0x00_4000	Delay Error Reg0
0x00_4001	Delay Error Reg1
0x00_4002	Delay Rate Reg0
0x00_4003	Delay Rate Reg1

VSI OUTPUT MODULE

0x00_5000	VSI Output Configuration Register

TIMING SUBSYSTEM

0x00_6000	RCLK PPS Rate Register
0x00_6001	System PPS Suppress Register

STATION UNIT BOCF GENERATOR

0x00_7000	Correlator Frame Length Reg0
0x00_7001	Correlator Frame Length Reg1

Station Unit Output Module

0x00_8000	SU Output Configuration Register

Test Vector Receiver Module

0x00_9000	TVR Sum Reg0
0x00_9001	TVR Sum Reg1
0x00_9002	TVR Bit to Sum Reg
0x00_9003	TVR Bias Reg0
0x00_9004	TVR Bias Reg1

The addresses above are internal to the DOM and are really 16-bit register locations. Though the addresses above increment by 1 between locations, this may not be so in the operating system, which typically increments a 16-bit register address by 2. However, the least significant bit from the PCI bus is dropped in making these internal addresses, so while the operating system addresses would increase by 2, the internal addresses will only increment by 1.One way of handling this address space is as an array of `shorts` in C with array location 0 at the DOM base address. Then let the operating system take care of the incrementing.

NOTE: Phase Calibration Tone Extraction and State Count system are located between 0x00_A000 and 0x00_A9FF in the DOM, if implemented (see DOM Known Register).

DOM REGISTER DESCRIPTIONS

GLOBAL REGISTERS

Address 0x00_0000: Enables Register

Enables the various blocks within the DOM.

Bit	Type	Name	Description
0	R/W	fpdp_xface_en	Enables the FPDP interface
1	R/W	strip_header_en	Enables the “strip header” module
2	R/W	unpack_xbar_en	Enables the unpack-xbar module. Also Phase Cal enable if implemented.
3	R/W	xbar_ram_en	Enables the post-xbar RAM
4	R/W	sdram_arbiter_en	Enables the SDRAM arbiter
5	R/W	sdram_core_en	Enables the SDRAM core functions
6	R/W	sdram_rcvr_en	Enables the SDRAM data receiver module
7	R/W	cfhr_en	Enables the Correlator Frame Header RAM module
8	R/W	delay_gen_en	Enables the Delay Generator module
9	R/W	vsio_en	Enables the VSI output module
10	R/W	suo_en	Enables the Station Unit output module
11	R/W	timing_en	Enables the Timing subsystem
12	R/W	bocf_gen_en	Enables the BOCF generation
13	R/W	tvg_en	Enables the Test Vector Generator
14	R/W	tvr_en	Enables the Test Vector Receiver
15	R	1	

Address 0x00_0001: Status Register

Provides some status of the DOM.

Bit	Type	Name	Description
0	R	header_err	Indicates a disk frame header error has occurred. Cleared by reseting the DOM.
1	R	DCM0	Indicates SDRAM DCM0 (board clock) has locked.
2	R	DCM1	Indicates SDRAM DCM1 (divided clock) has locked.
3	R	sdram_clk_stopped	Indicates that the SDRAM clk input has stopped. DOM should be reset.
7-4	R		0
8	R	sdram_init_done	Indicates the SDRAM has completed its initialization. 63999456 samples in buffer at end of init.
10-9	R	sdram_fill	00 – SDRAM buffer is 0% - 25% full. 01 – SDRAM buffer is 25% - 50% full. 01 – SDRAM buffer is 50% - 75% full. 11 – SDRAM buffer is 75% - 100% full.
11	R	sdram_buffer_empty	Indicates the SDRAM buffer is empty.
15-12	R	zero	tied to 0

Address 0x00_0002: ICLK Control

Control bits for the board "internal" clock. See data sheet for AD9850 clock generator.

Bit	Type	Name	Description
7-0	R/W	ICLK_data[7-0]	Internal clock data bits
8	R/W	ICLK_freq_update	Internal clock frequency update
9	R/W	ICLK_rst	Internal clock reset.
10	R/W	ICLK_wl_clk	Internal clock control clock

Address 0x00_0003: DOM Resets0

Resets for some DOM blocks.

Bit	Type	Name	Description
0	R/W	fpdp_xface_rst	FPDP interface reset.
1	R/W	fpdp_fifo_rst	FPDP receive FIFO reset.
2	R/W	strip_header_rst	Strip Header module reset
3	R/W	sh_fifo_rst	Post-Strip Header FIFO reset
4	R/W	unpack_xbar_rst	Unpack-Xbar reset. Also Phase Cal Reset (if implemented)
5	R/W	xbar_ram_rst	Post-Xbar RAM module reset
6	R/W	cfdr_rst	Correlator Frame Data RAM reset
7	R/W	cfhr_rst	Correlator Frame Header RAM reset
8	R/W	delay_gen_rst	Delay Generator reset
9	R/W	vsio_rst	VSI Output module reset.
10	R/W	suo_rst	Station Unit Output reset.
11	R/W	timing_rst	Timing subsystem reset.
12	R/W	bocf_gen_rst	BOCF generator reset.
13	R/W	tvg_rst	Test Vector Generator reset.
14	R/W	tvr_rst	Test Vector Receiver reset.

Address 0x00_0004: DOM Resets1

Resets for some DOM blocks.

Bit	Type	Name	Description
0	R/W	sdram_xface_rst	Resets the entire SDRAM control interface.
1	R/W	dcm_rst	Resets the SDRAM clocking subsystem.
2	R/W	fpdp_dcm_rst	Resets the FPDP DCM.

Address 0x00_0005: SDRAM Address0

Least significant bits of starting SDRAM read address used at next BOCF/VSI delay change.

Bit	Type	Name	Description
4-0	R/W	sdram_addr[4-0]	SDRAM starting read address. Corresponds to offset in sdram_rcvr's receive FIFO.
11-6	R/W	sdram_addr[11-6]	SDRAM starting read address. Corresponds to SDRAM column address.
15-12	R/W	sdram_addr[15-12]	SDRAM starting read address. Corresponds to lower 4 bits of SDRAM row address.

Address 0x00_0006: SDRAM Address1

Most significant bits of starting SDRAM read address used at next BOCF/VSI delay change.

Bit	Type	Name	Description
7-0	R/W	sdram_addr[23-16]	SDRAM starting read address. Corresponds to upper 8 bits of SDRAM row address.
9-8	R/W	sdram_addr[25-24]	SDRAM starting read address. Corresponds to SDRAM bank address.

Address 0x00_0007: DOM Known Register

A read only known value containing configuration information.

Bit	Type	Name	Description
15-8	R	known_val_reg[15-8]	Value = 0x5B
7	R	known_val_reg[7]	1 if DIM, 0 if DOM
6	R	known_val_reg[6]	1 if phase cal is implemented
5-0	R	known_val_reg[5-0]	Revision Code (DIM & DOM may differ)

Address 0x00_0008: DOM Scratch Register

A read/write scratch register for software.

Bit	Type	Name	Description
15-0	R/W	scratch_reg	Scratch register.

Address 0x00_0009: DOM Control Register

Control register for some DOM global functionality.

Bit	Type	Name	Description
1-0	R/W	back_end_mode[1-0]	Selects DOM mode. 00 – Station Unit 01 – VSI output 10 – TVG 11 - TVR
2	R/W	rclk_tristate_en	Tristates the RCLK output. Resets to '1'.
4-3	R/W	qspare[2 -1]	Software controllable qspare bits. qspare(2) = RESET# qspare(1) = DAV# to the serial links in SU mode.
5	R/W	dpsclk_source	Indicates source of dpsclk 0 - Use VSI DSPCLK connector 1 – Use "internal" clock on board
7-6	R/W	sw_led0	Controls the color of software LED0 00 – LED is off. 01 – LED is red. 10 – LED is green. 11 – LED is blue.
9-8	R/W	sw_led1	Controls the color of software LED1 00 – LED is off. 01 – LED is red. 10 – LED is green. 11 – LED is blue.

Address 0x00_000A: DOM Interrupt Mask Register

Interrupt Mask Register. A '1' written to a bit enables that interrupt.

Bit	Type	Name	Description
0	R/W	TOT_IM	Mask for TOT (Taken on Tick) interrupt.
1	R/W	DOM1PPS_IM	Mask for DOM1PPS interrupt.
2	R/W	CF_IM	Mask for Correlator Frame interrupt.
3	R/W	New_TVR_Sums_IM	Mask for New_TVR_Sum interrupt
4	R/W	ROT1PPS_IM	Mask for ROT1PPS interrupt.
5	R/W	PC_IM	Mask for Phase Cal interrupt (if implemented).

Address 0x00_000B: DOM Interrupt Register

Interrupt Register. Register is cleared on a read.

Bit	Type	Name	Description
0	INT	TOT_INT	TOT (Taken on Tick) interrupt. Marks reading of TOT bit from disk.
1	INT	DOM1PPS_INT	DOM1PPS interrupt. Marks DPS1PPS ticks
2	INT	CF_INT	Correlator Frame interrupt. Marks start of a new BOCF.
3	INT	New_TVR_Sums_INT	New_TVR_Sum interrupt. Indicates a new error weight and DC bias has been calculated by the TVR.
4	INT	ROT1PPS_INT	ROT1PPS interrupt. Marks system 1PPS (equivalent to ROT1PPS signal in VSI mode).
5	INT	PC_INT	Phase Calibration/State Count interrupt , if implemented.

Address 0x00_000C: DOM Correlator Frame Interrupt Counter

Counts the number of BOCFs since bocf_gen is first enabled.

Bit	Type	Name	Description
15-0	R	cf_cnt	Increments from 0 with each BOCF. Rolls over at fullscale.

STRIP HEADER MODULE

Address 0x00_1000: StreamStor Invalid Reg0

Lower half of the data word which indicates invalid data as marked by the SteamStor system. Resets to 0x55.

Bit	Type	Name	Description
15-0	R/W	ssi[15-0]	StreamStor invalid word, lower half

Address 0x00_1001: StreamStor Invalid Reg1

Upper half of the data word which indicates invalid data as marked by the SteamStor system. Resets to 0xAA.

Bit	Type	Name	Description
15-0	R/W	ssi[31-16]	StreamStor invalid word, upper half

Address 0x00_1002: DIM Invalid Reg0

Lower half of the data word which indicates invalid data as marked by the DIM. Can be the same as the StreamStor Invalid Reg0. Resets to 0x33.

Bit	Type	Name	Description
15-0	R/W	dimi[15-0]	DIM invalid word, lower half

Address 0x00_1003: DIM Invalid Reg1

Upper half of the data word which indicates invalid data as marked by the DIM. Can be the same as StreamStor Invalid Reg1. Resets to 0xCC.

Bit	Type	Name	Description
15-0	R/W	dimi[31-16]	DIM invalid word, upper half

Address 0x00_1004: Disk Frames per Second

Number of Disk Frames in 1 second of recorded time. This number is 1's based (i.e. a value of 100 indicates 100 disk frames per second, as opposed to a 0-based number which would indicate 101 frames per second.). Resets to 0x100.

Bit	Type	Name	Description
14-0	R	frames_per_sec[14-0]	Disk Frames per second.

Address 0x00_1005: Disk Frame VLBA Time Code0

Contains the 16 lsbs of the VLBA time code (word 1 of the Disk Frame Header) captured when the DOM's internal frame counter rolls over (frames_per_sec disk frames have been read off the disk). It is possible that this word could be marked invalid by the StreamStor.

Bit	Type	Name	Description
15-0	R	df_tc[15-0]	Disk Frame Time Code.

Address 0x00_1006: Disk Frame VLBA Time Code1

Contains the 16 msbs of the VLBA time code (word 1 of the Disk Frame Header) captured when the DOM's internal frame counter rolls over (frames_per_sec disk frames have been read off the disk). It is possible that this word could be marked invalid by the StreamStor.

Bit	Type	Name	Description
15-0	R	df_tc[31-16]	Disk Frame Time Code.

Address 0x00_1007: TOT Count

Set to 0 on reset, this counter increments every time the internal disk frame counter rolls over (i.e. every time frames_per_sec number of disk frames have been taken off the FPDP bus). The value rolls over at full scale. This is equivalent to the number of TOT_INTs which have occurred since FPDP accesses began, provided that the interrupt was enabled the entire time.

Bit	Type	Name	Description
15-0	R	tot_cnt[15-0]	TOT (Taken on Tick) Count

UNPACK XBAR REGISTERS

Address 0x00_2000 – 0x00_201F: Xbar Slice Setting RegN

These 32 5-bit registers control the crossbar (xbar) setting. The value should be the source mapping for the Nth bit of the Xbar output.. The xbar_slice_src value is the binary unsigned number from 0 to 31 which is the bit index of the input word to be mapped to output bit N. That is:

xbar_output(N) <= Xbar_input(xbar_slice_src);

Bit	Type	Name	Description
4-0	R/W	xbar_sliceN_src[4-0]	Bit index of Xbar input to be the source of Xbar output word bit N. Resets to N (i.e. Xbar is a thru).

Address 0x00_2020:

Unpack Code

Contains the Unpack Code indicating the Data Array Format (active bit streams per 32 bit word). An M bit stream data word format means that in a 32 bit StreamStor word there are 32/M actual data words each M bits long.

Bit	Type	Name	Description
2-0	R/W	unpack_code[2-0]	Unpack Code 000 – 32 bit stream data word format 001 – 16 bit stream data word format 010 – 8 bit stream data word format 011 –4 bit stream data word format 100 – 2 bit stream data word format 101 – 1 bit stream data word format
14-3		unimplemented	unimplemented
15	R/W	one_bit_samples	Should be set if data encoding on disk uses one-bit samples. Cleared if using two-bit samples.

CORRELATOR FRAME HEADER RAM BANK

Address 0x00_3000 – 0x00_30EF:

Correlator Frame Header RAM Bank A

The Correlator Frame Header RAM (CFHR) Bank A hold the 240 16-bit correlator frame header words for the 1st, 3rd, 5th, … correlator frames. This should be pre-loaded prior to station unit output being triggered. Each of the 16 bits in a RAM location maps to a magnitude output bit stream. This RAM should be updated after CF_INTs 2,4,6,8,... .

Bit	Type	Name	Description
15-0	R/W	cfhrA[15-0]	Correlator Frame Header words.

Address 0x00_3100 – 0x00_31EF:

Correlator Frame Header RAM Bank B

The Correlator Frame Header RAM (CFHR) Bank B hold the 240 16-bit correlator frame header words for the 2nd, 4th, 6th, … correlator frames. This should be pre-loaded prior to station unit output being triggered. Each of the 16 bits in a RAM location maps to a magnitude output bit stream. This RAM should be updated after CF_INTs 3,5,7… .

Bit	Type	Name	Description
15-0	R/W	cfhrB[15-0]	Correlator Frame Header words.

DELAY GENERATOR

Address 0x00_4000 : Delay Error Reg0

This register is written with the lower half of the delay error (a 32-bit unsigned number). It should be written to prior to output triggering and after every CF_INT. Resets to 0x0000.

Bit	Type	Name	Description
15-0	R/W	del_err[15-0]	LSBs of the 32-bit unsigned number indicating the delay error associated with the next Correlator Frame.

Address 0x00_4001 : Delay Error Reg1

This register is written with the upper half of the delay error (a 32-bit unsigned number). It should be written to prior to output triggering and after every CF_INT. Resets to 0xFFF0

Bit	Type	Name	Description
15-0	R/W	del_err[31-16]	MSBs of the 32-bit unsigned number indicating the delay error associated with the next Correlator Frame.

Address 0x00_4002 : Delay Rate Reg0

This register is written with the lower 16 bits of the delay rate (an 18-bit unsigned number). It should be written to prior to output triggering and after every CF_INT. Resets to 0xFFFF.

Bit	Type	Name	Description
15-0	R/W	del_rate[15-0]	LSBs of the 32-bit unsigned number indicating the delay rate associated with the next Correlator Frame.

Address 0x00_4003 : Delay Rate Reg1

This register is written with the upper 2 bits of the delay rate (an 18-bit unsigned number). It should be written to prior to output triggering and after every CF_INT. This also contains the delay generator mode bit which is also updated every CF_INT. Resets to 0x0003.

Bit	Type	Name	Description
1-0	R/W	del_rate[17-16]	MSBs of the 18-bit unsigned number indicating the delay rate associated with the next Correlator Frame.
14-2		unimplemented	unimplemented
15	R/W	del_gen_mode	Delay Generator Mode Bit 0 – Repeat output of last data word on Delay Adder Carry Out. 1 – Skip output of next data word on Delay Adder Carry Out.

VSI OUTPUT MODULE

Address 0x00_5000 : VSI Output Configuration Register

Configures the VSI Output module.

Bit	Type	Name	Description
2-0	R/W	vsi_prescl_code[2-0]	Controls the baud rate of the data output in VSI mode relative to the RCLOCK frequency. 000 – Output data baud = RCLK freq. 001 - Output data baud = RCLK freq/2 010 – Output data baud = RCLK freq/4 011 – Output data baud = RCLK freq/8 100 - Output data baud = RCLK freq/16
14-3		unimplemented	unimplemented
15	R/W	vsio_run	VSI Output Run bit. 1 – start output on next unsuppressed system 1PPS. 0 – stop output on next unsuppressed system 1PPS. This is useful for back-to-back scans without emptying the RAM buffer.

Address 0x00_6000 : RCLK PPS Rate Register

Configures the RCLOCK and the system 1PPS.

Bit	Type	Name	Description
2-0	R/W	rclk_rate_code[2-0]	Controls the division of the dpsclk (or board "internal" clock) in the generation of rclk. 000 – RCLK freq = DPSCLK freq 001 – RCLK freq = DPSCLK freq/2 010 – RCLK freq = DPSCLK freq/4 011 – RCLK freq = DPSCLK freq/8 100 – RCLK freq = DPSCLK freq/16
5-3		PPS_div_code[2-0]	Controls how many DPSCLK cycles per 1PPS. 000 – 128 million DPSCLKs per PPS. 001 – 64 million DPSCLKs per PPS 010 – 32 million DPSCLKs per PPS 011 – 16 million DPSCLKs per PPS 100 – 8 million DPSCLKs per PPS 101 – 4 million DPSCLKs per PPS 110 – 2 million DPSCLKs per PPS 111 – 100 DPSCLKs per PPS (for testing only).
6	R/W	use_internal_pps	Controls the source of the 1PPS start trigger. 0 – the DPS1PPS will trigger the start of the PPS divider/generator. 1 – enabling the timing subsystem will trigger the start of the PPS divider/generator (for use when there is no DPS1PPS).

Address 0x00_6001 : System PPS Suppress Register

Controls the suppression of the DOM internal 1PPS pulse which is used to trigger several blocks. An unsuppressed 1PPS will load a new SDRAM read starting address in VSI mode (to change the delay), and begin output from the VSI Output module or SU Output module. In TVG or TVR mode an unsuppressed 1PPS will begin test vector processing.

Bit	Type	Name	Description
0	R/W	suppress_pps	1 – Suppress generation of internal 1PPS. 0 – Allow internal 1PPS. Resets to 1.

STATION UNIT BOCF GENERATOR

Address 0x00_7000 : Correlator Frame Length Reg0

Lower 16 bits of the29-bit, 0-based word which indicates the correlator frame data payload length in Station Unit mode. Length is measured in RCLKs

Bit	Type	Name	Description
15-0	R/W	cf_payload_len[15-0]	LSBs of number of RCLKs (24-bits wide) in a CF data payload.

Address 0x00_7001 : Correlator Frame Length Reg1

Upper 16 bits of the 29-bit, 0-based word which indicates the correlator frame data payload length in Station Unit mode. This also contains the BOCF length code.

Bit	Type	Name	Description
12-0	R/W	cf_payload_len[31-16]	MSBs of number of RCLKs (29-bits wide) in a CF data payload.
15-13	R/W	bocf_code[2-0]	Indicates the length of a BOCF 000 – BOCF is 240 RCLK cycles 001 – BOCF is 480 RCLK cycles 010 – BOCF is 960 RCLK cycles 011 – BOCF is 1920 RCLK cycles 100 – BOCF is 3840 RCLK cycles

STATION UNIT OUTPUT MODULE

Address 0x00_8000 : SU Output Configuration Register

Configures the SU Output module.

Bit	Type	Name	Description
3-0	R/W	suo_prescl[3-0]	suo_prescl is an unsigned, 4-bit terminal count for a zero based counter in the station unti output. This counter increments every RCLK cycle and when it reaches suo_prescl, the counter rolls over to zero and a new data word is placed on the output pins. This is similar to vsi_prescl_code. The only valid values are 0000, 0001, 0011, 0111, or 1111.
14-4		unimplemented	unimplemented
15	R/W	suo_run	Similar to the vsio_run bit: 1 – start Station Unit output at next BOCF. 0 – stop Staiton Unit output at next BOCF.

TEST VECTOR RECEIVER MODULE

Address 0x00_9000 : TVR Sum Reg0

Lower 16 bits of the 32-bit number indicating the error weight (number of incorrect bits) occurring on the bit indicated by tvr_bit2sum in 1 TOT second.

Bit	Type	Name	Description
15-0	R	tvr_sum[15-0]	Lower 16 bits of TVR error weight sum.

Address 0x00_9001 : TVR Sum Reg1

Upper 16 bits of the 32-bit number indicating the error weight (number of incorrect bits) occurring on the bit indicated by tvr_bit2sum in 1 TOT second.

Bit	Type	Name	Description
15-0	R	tvr_sum[31-16]	Upper 16 bits of TVR error weight sum.

Address 0x00_9002 : TVR Bit to Sum Reg

Index of the data bit to process in the TVR. Can be changed every NEW_TVR_SUM_INT.

Bit	Type	Name	Description
4-0	R	tvr_bit2sum[4-0]	Index in binary (0 -31) of data bit to process (calculate error totals and DC bias) in the TVR.

Address 0x00_9003 : TVR Bias Reg0

Lower 16 bits of the 32-bit, 2's complement number indicating the DC Bias of the bit indicated by tvr_bit2sum in 1 TOT second.

Bit	Type	Name	Description
15-0	R	tvr_bias[15-0]	Lower 16 bits of TVR dc bias.

Address 0x00_9004 : TVR Bias Reg1

Upper 16 bits of the 32-bit, 2's complement number indicating the DC Bias of the bit indicated by tvr_bit2sum in 1 TOT second.

Bit	Type	Name	Description
15-0	R	tvr_bias[31-16]	Upper 16 bits of TVR dc bias.