Phase Calibrator Module

A Functional Description.
(including address map)

Overview

Figure 2 shows a block diagram for the PCM.

The board is accessed by the SUCC via the VME bus connected through PL2. Signals for processing arrive via PL1.

The VME interface is an idt device in harness with AMD MACH PLD. The data signal interface is a pair of Xilinx FPGAs.

The core of the functionality is the 144 accumulators (counters) that are located in eight Xilinx FPGAs (18 per). Seven of these devices are slaves, one a master that holds the control logic for the accumulation process. The sign, magnitude and validity of the 16 data signals (called channels) are used to read data from the pre-loaded SRAMs for each channel. The pre-loading of the SRAMs is achieved using a different set of programmes for these Xilinx devices.

A micro-processor and associated memory is used to control the programme of the Xilinx FPGAs; the commencement of the counting and the processing of the resultant counts back to the SUCC.

Operational status and Xilinx programmed DONE bits from the FPGAs are passed via an interface to front panel LEDs.

Microprocessor and VME interface

The VME interface is implemented in an AMD EPLD. Messages to and from the Station Unit Control Computer (SUCC) are placed in a Dual Ported RAM. The Dual Ported RAM is shared with the Microcontroller via a common address and data bus that also communicates with the Xilinx devices; comms ports and LEDs. The Micro loads each of the SRAMs via the FPGAs with the phase cal. tables from the SUCC in write-verify mode and controls the starting, stopping and reading of the counters in accumulation mode.

The counters are implemented in Xilinx FPGA's which are programmed by the Micro. The master FPGA is programmed in asynchronous peripheral mode, the slaves and the data register FPGAs are programmed in serial-parallel mode from the master (see fig 1). The master and slaves have different configurations in the two operation modes: Write-verify and accumulation.

The local micro controller (MC68340) has two serial ports. Both of these are brought out, at RS232 levels, to the front panel 48 way DIN41612 connector, SK1. During development this has been used as a diagnostic port, along with the test points from the master FPGA.

The micro controller can also be run in Background Debug Mode (BDM) via a special port which is brought out to PL3 (and also SK1). This has been used in development as a means of loading and running software at source level.

The control of address decode to provide direction and enable signals for access to the micro controller's address and data busses is also performed in the AMD EPLD device. An address map for the pcb, (not the internal operation of the micro controller) is attached in appendix A.

Write-Verify mode

This mode is used to load the SRAMs with the phase cal tables that are kept in the SUCC. It is used solely for writing to and verifying the contents of the SRAMs. During development and testing it is also used to confirm the integrity of the hardware.

The channel clock and the associated high speed control lines and the data are disabled in this mode. Transfers are synchronised to a 16 MHz clock.

Accumulation Mode

This mode is used to count the contents of the SRAMs dependent upon the incoming data. Within this mode there are three distinct operations: The initialisation of the counting; the actual accumulation phase, and the reading of the counters.

The initialisation phase consists of resetting all the accumulators which is achieved by globally resetting the master and slave FPGAs; writing the start address to the master FPGA, and receiving CFRAME (channel frame) after the first rising edge of SOT (second of tot). With these conditions met the next phase can start.

The accumulation phase causes all 144 accumulators to count under control of the channel clock (CCLK), CFRAME, and the 16 channels of data; sign, magnitude and validity (s, m, v). The channel data forms the high three address lines for the SRAMs, the lower twelve address lines are from a 3200 bit counter in the master FPGA. The data from each of the 8 data lines of the SRAMs is gated with CFRAME and each resultant high is added to an accumulator for each data line. The gated validity line is treated in the same way. Each accumulator is 32 bits long, and should be read every 134 seconds to ensure no overflow at 32 Mbits/s. The inter frame gaps are monitored in the master FPGA and these gaps send an interrupt to the micro. The accumulation phase can be halted at any of these gaps. The micro keeps a tally of all the interrupts so that the number of frames (and hence the number of bits) can be reported to the SUCC.

The reading of the counters can only be done with the counting inhibited. The accumulators have to be read by the micro in two sixteen bit words.

Channel Data physical.

The following table gives the Xilinx FPGA and SRAM used for each channel.

Channel No	I/P pin (PL1) (s,m,v)	Data reg I/P (s,m,v)	Data reg O/P (s,m,v)	Cct ref. of Xilinx	Cct ref. of SRAM
1	A10,A11,A12	U61-25,26,29	U61-60,50,46	U26	U27
2	B9,B11,B12	U61-38,18,28	U61-51,58,47	U26	U28
3	C10,C12,C13	U61-24,17,20	U61-61,59,56	U23	U24
4	D9,D10,D11	U61-23,39,27	U61-62,49,48	U23	U25
5	E10,E11,E12	U61-15,16,19	U61-67,65,57	U35	U36
6	A13,A15,A16	U61-14,10,U62-28	U61-68,66,U62-48	U35	U37
7	B13,B14,B16	U61-6,9,U62-27	U61-80,77,U62-49	U20	U21
8	C14,C15,C17	U61-5,8,U62-26	U61-81,78,U62-50	U20	U22
9	D13,D14,D15	U61-4,7,U62-38	U61-82,79,U62-51	U17	U18
10	E14,E15,E16	U61-3,U62-39,25	U61-83,U62-47,66	U17	U19
11	A17,A18,B17	U62-29,16,24	U62-46,60,67	U29	U30
12	B18,B19,C18	U62-20,15,14	U62-56,61,62	U29	U31
13	C19,C20,D16	U62-19,9,23	U62-57,65,68	U32	U33
14	D18,D19,D20	U62-18,8,5	U62-58,78,81	U32	U34
15	E17,E19,E20	U62-17,7,4	U62-59,79,82	U58	U59
16	D21,E21,E22	U62-10,6,3	U62-77,80,83	U58	U60

Fig 1. Xilinx configuration diagram.

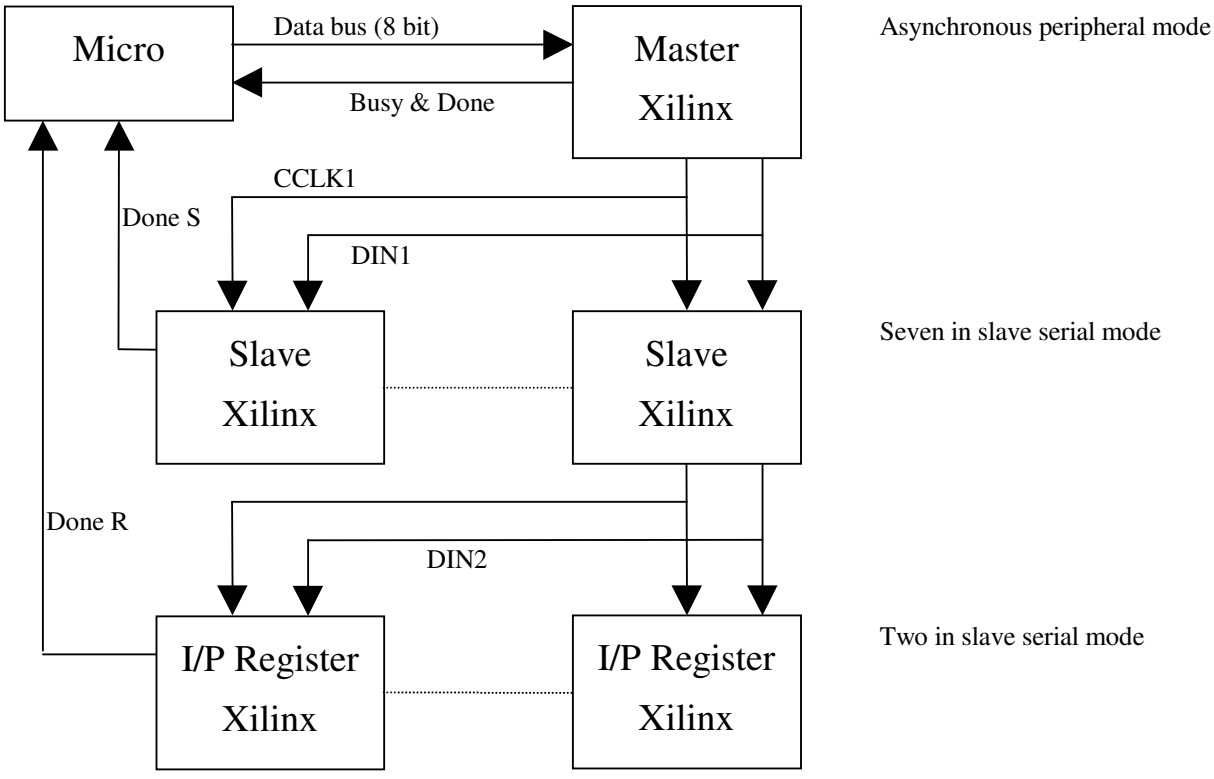
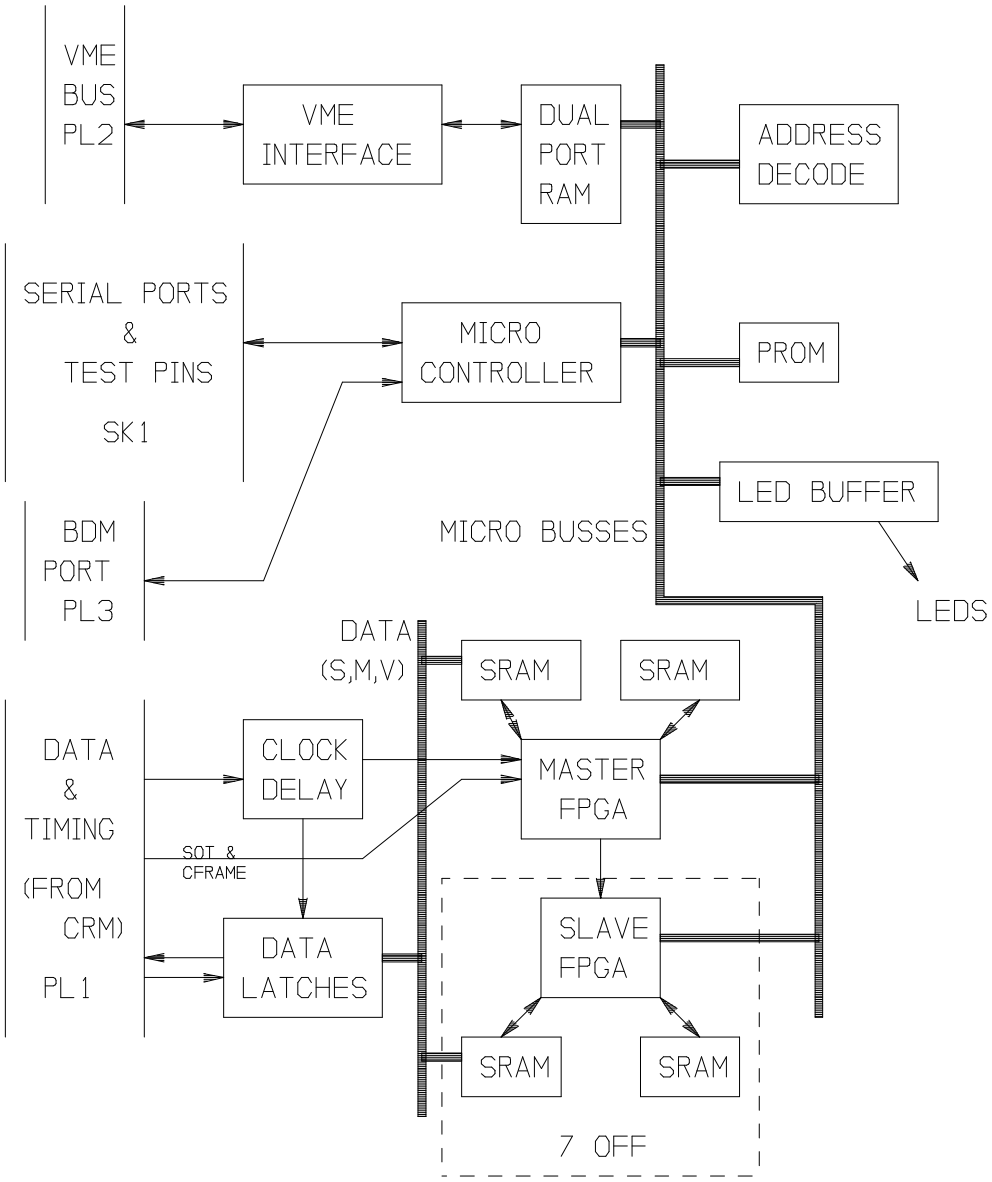
Figure 1 Block Diagram for the PCM card