Delay Control Module (DCM)

Introduction

The functions of the DCM are to control the partitioning of channel data into correlator frames, to control the channel delay or advance from the Delay Memory Module (DMM), to facilitate the synchronisation of ROT based timing with the received system tick. Operation is described with reference to the block diagram.

Connectors

There are two connectors which interface to the back plane of the station unit rack. They are designated PL1 and PL2. PL1 is a standard 96 pin VME bus connector. PL2 is a 185 pin connector which carries all other relevant station unit signals. There is a 48 pin connector on the front panel which carries the RS232 serial link and background debug mode (BDM) signals for the microcontroller. Some test signals are also present. The pin connections can be found on the circuit diagrams.

VME Interface

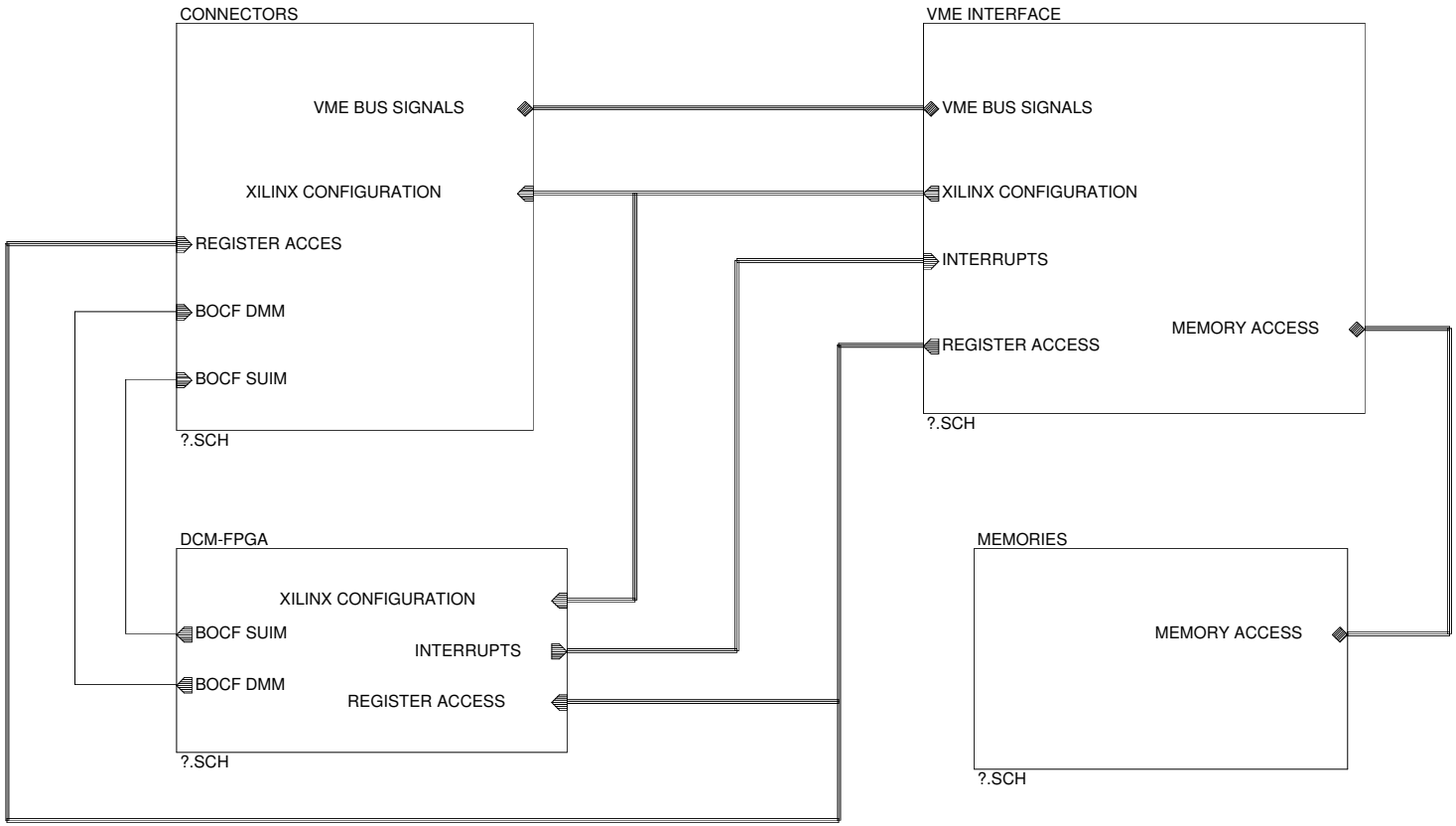
This block consists of the microcontroller, dual port RAM, one programmable logic device for VME control signals, one programmable logic device for XILINX control signals, and associated 'glue logic' devices. Software for the microcontroller sets up the module for operation. The station unit computer (SUCC) communicates with the DCM microcontroller via a messaging system based on the dual port RAM. The microcontroller also controls the DMMs via connector PL2. At switch on and when requested by the SUCC, the DCM XILINX gate array is first configured and registers initialised, then the DMM XILINX gate arrays are configured and registers initialised. The microcontroller receives interrupts from the DCM gate array. The source of the an interrupt within the gate array must be read from a gate array register (see 1660010015).

Memories

The firmware is held in two 128 Kbytes flash ROMs and other memories are two 128 Kbytes static RAMs. Various 'glue logic' devices ensure correct access to these memories.

DCM-FPGA

This block is a XILINX gate array, the only on one the DCM (see 1660010015. It performs the functions of generating a beginning of correlator frame (BOCF) signal and interrupts to monitor ROT based timing. It also provides a hardware translator for the manipulation of data which is inserted into the correlator frame header. There are two redundant sections of the gate array which have not been removed. The first is a test 1 Hz output (TEST_SYSTICK_DM) when station clock is 32 MHz . The second is a dead reckoned estimate of the current receive address in the delay memory (this has never been used). There are two BOCF outputs, one for the SUIM and one for the DMM.



DELAY CONTROL MODULE

BLOCK DIAGRAM

1660010015

This description should be read in conjunction with the circuit diagrams for the gate array. Signal names which are used are those found in the diagrams. General principles of operation are described and no detail of implementation to gate level is given.

The FPGA is set-up and controlled from the DCM microcontroller (sheets 3,4,7,11). This communicates via sixteen bi-directional data lines and decoded address and read/write control signals. The decoded signals select registers for writing and multiplexers for reading. Eight outputs, LED2G to LED5G, and LED2R to LED5R, provide the means for software control of four tri-colour LED's on the front panel of the DCM (sheet 6).

TEST_SYSTICK_DM is generated by dividing STNCLK by thirty two million (sheet 5). The output is high for sixteen thousand clock periods. Hence when station clock is 32 MHz, TEST_SYSTICK_DM is a 0.5ms. pulse at 1 Hz. At other station clock frequencies these figures will be scaled proportionally.

The current receive address is dead reckoned by clocking a counter by CHANNEL_CLOCK while enabled by CHANNEL_FRAME (sheet 12). This is a twenty three bit counter whose current count can be read by the micro-controller at two defined addresses. A write to these addresses will clear the counter. This circuit has not been tested. The facility has never been used because the function is implemented on a per channel basis on the DMM boards.

The hardware translator (sheet 2) must be used in the correct sequence. This is, eight bytes of data are sequentially written to eight registers. Corresponding bits across these input bytes constitute the translated data. These are read out sequentially after all eight input registers have been loaded.

Five signals can generate an interrupt to the micro-controller (sheet 9):-
ROT_INT
BOCFINT
SOTINT
SYSTICK_INT
ROVERINT
These are individually enabled or disabled by a mask register which is written by the micro-controller. The source of an interrupt is determined from a status register which is read by the micro-controller.

ROVERINT is generated by an overflow from the unused delay memory receive address counter. This is never used.
SYSTICK_INT is generated from the SYSTEMTICK input. This is the systick received from the SUIM via the rack backplane.
SOTINT is generated from the SOT input. This is the second of tot signal received from the CRM via the rack backplane.
BOCFINT is generated from the BOCF signal which generated within this FPGA.
ROT_INT is generated from the ROT counter within this FPGA.

The ROT counter is a twenty four bit binary down counter (sheet 8). Any binary value up to the twenty four bits can be pre-set into the counter from a register which is written to by the micro-controller. The counter is clocked by STNCLK and at terminal count the pre-set value is reloaded. Terminal count also generates ROT_INT. Hence the ROT counter can be made to generate interrupts at a pre-defined rate per second. SYSTICK also causes the pre-set value to be loaded into the counter which resynchronises the counter every second. At this same time the count remaining is latched into a register which is read by the micro-controller.

The generation of BOCF is determined by register values written by the micro-controller (sheet 10). The length of the BOCF signal, the header length, is set by H_LENGTH_DATA which is sixteen bits wide. The header length count can be repeated a number of times set by the value in H_MUL_DATA which is eight bits wide. The period between BOCF headers is set by C_FRM_LEN_DATA which is thirty two bits wide. All the counters which generate BOCF are clocked by STNCLK. Hence the length of the BOCF header and the BOCF repetition rate can be set in terms of the number of station clocks. The BOCF header length is (H_LENGTH_DATA * H_MUL_DATA) station clocks. The BOCF repetition rate is ((H_LENGTH_DATA * H_MUL_DATA) + C_FRM_LEN_DATA) station clocks.

The start of the first BOCF header from a stopped condition can be delayed as set by C_FRM_USO_DATA, which is eight bits wide, and TX_ST_OFF_DATA, which is thirty two bits wide. The generation of the BOCF signal is stopped when the low order word of TX_ST_OFF_DATA is written to the register. If both these registers are zero, the first BOCF starts at the next systick after that write. Any non zero value in C_FRM_USO_DATA delays the start of the first BOCF by that number of systicks. Any non zero value in TX_ST_OFF_DATA delays the start of the first BOCF by that number of station clocks from the expiry of the C_FRM_USO_DATA delay. Hence, the start of the first BOCF can be delayed by C_FRM_USO_DATA systicks plus in TX_ST_OFF_DATA station clocks from the synchronising systick.

BOCF drives two outputs. BOCF_DM is used only within the DCM, PCM, and DMM boards. BOCF_SU is a delayed version of BOCF which is routed to and only used in the SUIM board.