Channel Recovery Module (CRM)

Introduction

The function of the CRM is to accept track signals from the Track Recovery Modules (TRMs) and reconstitute channel signals. Operation is described with reference to the block diagram. The blocks in this diagram were extracted from the circuit diagrams. However, these circuits are not described in detail.

Connectors

There are two connectors which interface to the back plane of the station unit rack. They are designated PL1 and PL2. PL1 is a standard 96 pin VME bus connector. PL2 is a 185 pin connector which carries all other relevant station unit signals. There is a 48 pin connector on the front panel which carries the RS232 serial link and background debug mode (BDM) signals for the microcontroller. Some test signals are also present. The pin connections can be found on the circuit diagrams.

VME Interface

This block consists of the microcontroller, dual port RAM, two programmable logic devices for VME control signals and XILINX control signals, and associated 'glue logic' devices. Software for the microcontroller sets up the module for operation. The station unit computer (SUCC) communicates with the CRM microcontroller via a messaging system based on the dual port RAM. At switch on and when requested by the SUCC, the XILINX gate arrays are configured and registers initialised. For configuration the XILINX gate arrays are daisy-chained. Also at this time the cross-bar switch is written with default (one to one) input to output data. During a scan the sole function of the micrcontroller is to monitor the end of track frames and write new data to the cross-bar switch.

Memories

The firmware is held in two 128 Kbytes flash ROMs and other memories are two 128 Kbytes static RAMs. Various 'glue logic' devices ensure correct access to these memories.

Clocks Generator

This block is a XILINX gate array (see 1660010010). It is the first gate array in the daisy-chain. Track Clock and Channel Clock frequencies are selected and generated by this device. It also generates the Track Frame signal. This is routed to the TRMs through the rack back plane. A delayed version is used on board in other gate arrays. The delay is equal to the total pipeline delay of track signals arriving from the TRMs. The selection of multiplex or de-multiplex ratio and one or two bit data is stored in this gate array. These data are passed on to the MUX/DEMUX block.

Input Buffers

Track signals are routed from the connector PL2 and clocked into register buffers by Track Clock. There are sixty four track signals. The outputs from the buffers are routed to the Cross Track Parity block.

Cross Track Parity

This block is a XILINX gate array (see 1663010010). It is the last gate array in the daisy-chain. The main function of this gate array is no longer required. The mode is selected to pass track signals through with an inevitable pipeline delay. It also generates a marker signal which locates the position of the validity bit within the track signals data. The track signals are

routed to the Barrel-Unroll block. The marker signal is routed to the Validity Bit Stream block.

Barrel-Unroll

This block is a 64 x 64 cross bar switch. Any of sixty four inputs can be routed to any of sixty four outputs. It is used in a mode where a new configuration can be written to the device but this is only transferred to the outputs on receipt of a load command. At the end of every track frame the next set of switch configurations are loaded to the outputs and the microcontroller starts writing the set for the next track frame. In this way barrel rolling of track signals can be reversed. If there is no barrel rolling to be reversed the same set of switch configurations is written at the end of every track frame. The outputs of the cross bar switch are routed to the Validity Bit Stream block.

Validity Bit Stream

This block is two XILINX gate arrays (see 1662010010). They are configured identically in parallel but third in the gate array daisy chain. Each gate array processes thirty two track signals. The validity bits, which are identified by the marker signal, are used to generate a parallel validity signal for each track signal. The original validity bits in the track signals are forced to logic zero. The corresponding bits in the validity signal are also logic zero. The track and validity signals are routed to the MUX/DMUX block.

MUX/DMUX

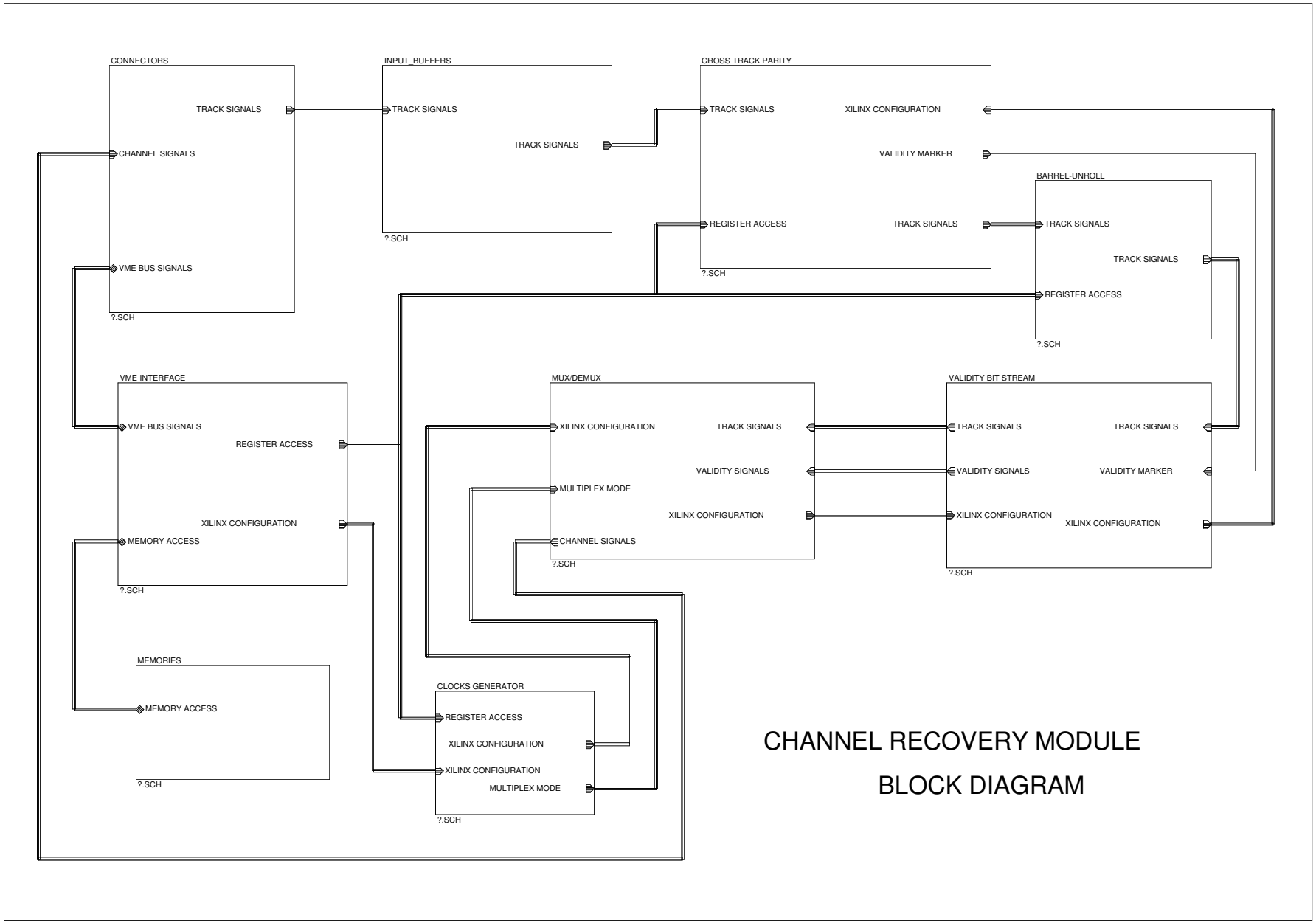
This block is a XILINX gate array (see 1661010010 and 1664010010). It has two configurations depending in which modes it is required to operate. It is the second gate array in the daisy-chain. There are five main modes of operation. In addition each mode can operate as one bit data or two bit data. The modes are:-

MODE	FUNCTION	DATA
mux1_4	4 tracks into 1 channel signal	one bit
mux1_4	4 tracks into 1 channel signal	two bit
mux1_2	2 tracks into 1 channel signal	one bit
mux1_2	2 tracks into 1 channel signal	two bit
mux1_1	1 track into 1 channel signal	one bit
mux1_1	1 track into 1 channel signal	two bit
mux4_1	1 track into 4 channel signals	one bit
mux4_1	1 track into 4 channel signals	two bit
mux2_1	1 track into 2 channel signals	one bit
mux2_1	1 track into 2 channel signals	two bit

Each channel consists of three channel signals Sign, Magnitude, and Validity. In one bit data modes, the Magnitude signal is forced to logic one. The Validity signal of a channel is the logical and of the validity signals of the tracks which constitute the channel. Sixteen channels (48 channel signals) are generated. The channel outputs are routed to the Connectors block.

CRM Gate Arrays

These descriptions should be read in conjunction with the circuit diagrams for the various gate arrays. Signal names which are used are those found in the diagrams. General principles of operation are described and no detail of implementation to gate level is given.


CONNECTORS
TRACK SIGNALS
CHANNEL SIGNALS
VME BUS SIGNALS
?.SCH
INPUT_BUFFERS
TRACK SIGNALS
TRACK SIGNALS
?.SCH
CROSS TRACK PARITY
TRACK SIGNALS
XILINX CONFIGURATION
VALIDITY MARKER
REGISTER ACCESS
TRACK SIGNALS
?.SCH
BARREL-UNROLL
TRACK SIGNALS
TRACK SIGNALS
REGISTER ACCESS
?.SCH
VME INTERFACE
VME BUS SIGNALS
REGISTER ACCESS
XILINX CONFIGURATION
MEMORY ACCESS
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MUX/DEMUX
XILINX CONFIGURATION
TRACK SIGNALS
VALIDITY SIGNALS
MULTIPLEX MODE
XILINX CONFIGURATION
CHANNEL SIGNALS
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VALIDITY BIT STREAM
TRACK SIGNALS
TRACK SIGNALS
VALIDITY SIGNALS
VALIDITY MARKER
XILINX CONFIGURATION
XILINX CONFIGURATION
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MEMORIES
MEMORY ACCESS
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CLOCKS GENERATOR
REGISTER ACCESS
XILINX CONFIGURATION
XILINX CONFIGURATION
MULTIPLEX MODE
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CHANNEL RECOVERY MODULE
BLOCK DIAGRAM

1660010010 (CLKGEN)

This FPGA generates control and clock signals. A 75 MHz input clock drives a seven stage divider chain to produce the following frequencies:-

37.5 MHz
18.75 MHz
9,375 MHz
4.6875 MHz
2.34375 MHz
1.171875 MHz
0.5859375 MHz

Channel Clock can be selected from any of these frequencies. Track Clock can be selected from 18,75 MHz, 9.375 MHz, 4.6875 MHz, 2.34375 MHz. The actual selection required is determined by data FSELCODE from a register which is written into from the CRM microcontroller. This register also holds data MXC which is output from this gate array to set the multiplexing or demultiplexing ratio.

There are other registers which control the generation of Track Frame and Second of TOT (SOT) signals. Communication from and to the microcontroller is via an eight bit bi-directional port. Address lines, select and write signals are inputs to the FPGA.

The number of Track Clocks per Track Frame is pre-set at 22500. The number of Track Clocks between Track Frames is set in register RTFRM. The actual number Track Clocks is the value in RTFRM + 2. Register NTFRM originally defined the number of Track Frames to be transferred, the actual number being the value in NTFRM + 1. The NTFRM function is now disabled but the circuitry has not been deleted.

The number of Track Frames per SOT is set in register RSOT. The actual value is the value in RSOT except for a value of zero which gives an actual value of 2E+10. Register SSOT originally set a delay, in Track Frames, before the first SOT was generated. The actual delay being the value in SSOT except for a value of zero which gives an actual value of 2E+10. The SSOT function is now disabled but the circuitry has not been deleted.

At the end of the Track Frame period a control signal for the barrel roll cross bar switch is generated. This is Ored with an input signal XBARLD_OUT to produce an output signal XBARLD_IN. This causes the cross bar switch to transfer any previously loaded switch set-up to its outputs. At the same time a signal XBAR_INT is set active low. This signals to the microcontroller that new cross bar switch data should be written. This signal is cleared by the input signal XBARWR.

1663010010 (CTP)

The cross track parity correction circuits are untested and are forced into a not selected state by a write to the control register. Hence the operation of these circuits will not be described. The control register is written to and read from via bi-directional port XD. This is under the control of signals XRW and XSEL. CTP_MODE and HEADER_MODE set to logical zero disables the cross track parity function.

TRACK_FRAME is clocked in and delayed by TRACK_CLOCK. This synchronises a divide by nine counter. The output of this counter is validated by the delayed TRACK_FRAME to generate the output signal VCLK. VCLK marks the position of the validity bit in the TRACK signals.

TRACK data is clocked in by TRACK_CLOCK. DTRACK passes through the combinatorial logic unaltered and TRACK_OUT is clocked out by TRACK_CLOCK.

A waveform diagram illustrating validity bit marking is shown in Figure 1.

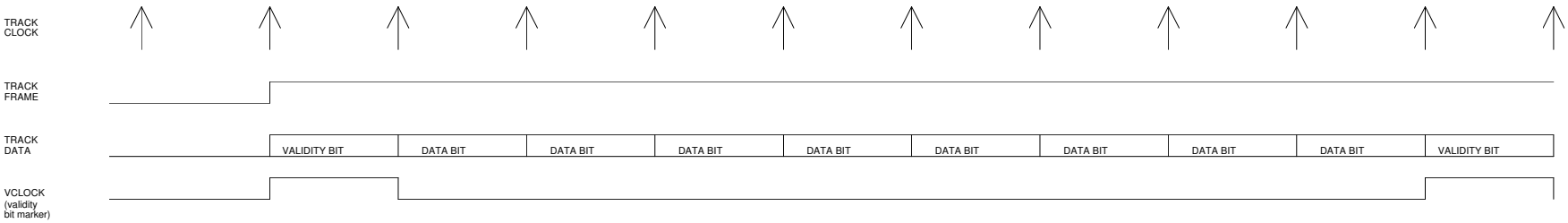

Figure 1. VALIDITY BIT MARKING (pipeline delays not shown)

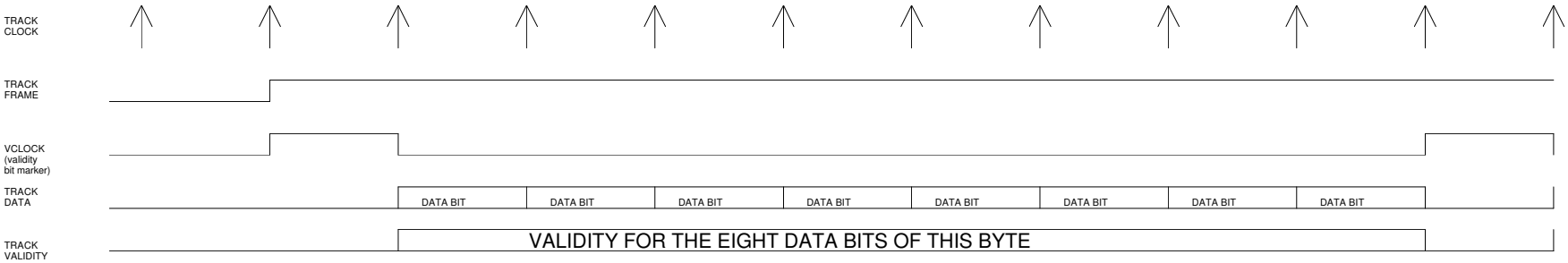

Figure 2. VALIDITY BIT EXTRACTION (pipeline delays not shown)

1662010010 (VBIT)

This FPGA extracts the value of the validity bit in the data and generates a parallel validity signal which reflects that value for the remaining 8 bits of the byte. The original position of the validity bit in the data is set to logic zero. The corresponding bit position in the validity signal is also set to logic zero.

TRK_IN, TRACK_FRAME, and VCLK are clocked in by TCLK. VCLK is a signal in parallel with the track data TRK_IN which marks the position of the validity bit in the data. TRK_IN signals are clocked into serial to parallel shift registers. A delayed version of VCLK (DVCLK) loads the parallel data into an eight bit parallel to serial shift register and the validity bit into a one bit register. Data and validity are clocked out of these registers by TCLK. DVCLK also forces the data and validity signals to be zero.

TRACK_FRAME is delayed to correspond with the pipeline delays introduced to the data (D_TRACK_FRAME) and DVCLK is further delayed (DDVCLK) to match this. CHANNEL_DATA, VALIDITY, D_TRACK_FRAME, and DDVCLK are clocked out by TCLK. A signal CCLK is generated and output as a test signal but has no part in the operation of the CRM..

A waveform diagram illustrating validity bit extraction is shown in Figure 2.

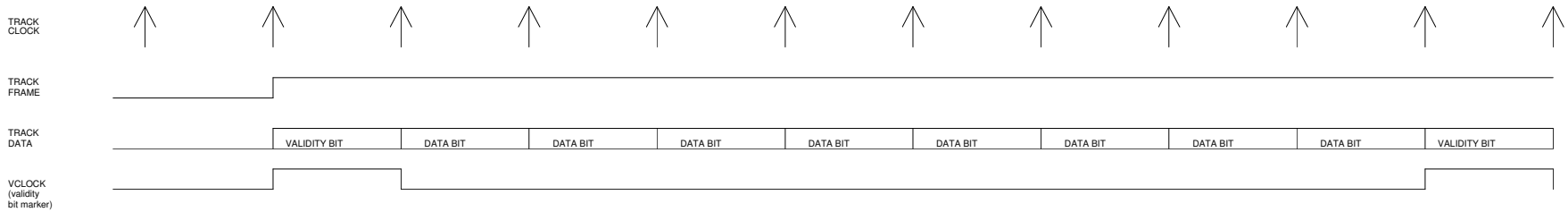

Figure 1. VALIDITY BIT MARKING (pipeline delays not shown)

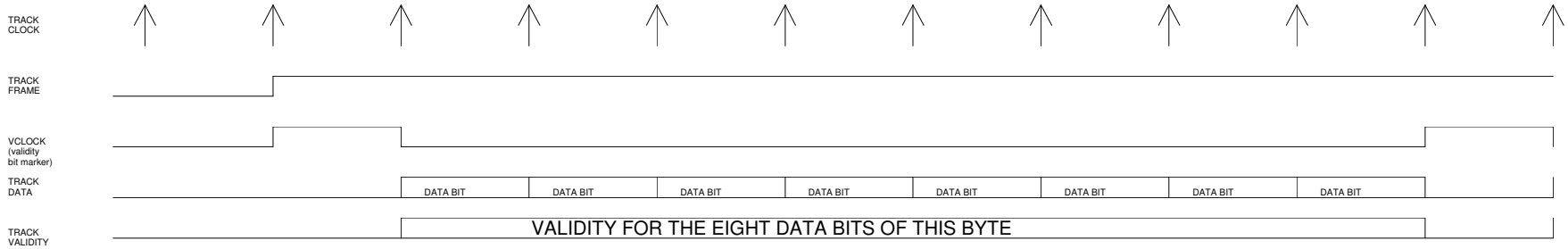

Figure 2. VALIDITY BIT EXTRACTION (pipeline delays not shown)

1661010010 (MMUX)

This FPGA implements the 1:1, 2:1, and 4:1 multiplexing modes. That is one input track to one output channel, two input tracks to one output channel, and four input tracks to one output channel. In these modes, Channel Clock frequency is always equal to or greater than Track Clock frequency.

TRACK_DATA, VALID_IN, TRACK_FRAME, T_REF_SOT, and DDVCLK are clocked in by TRACK_CLOCK. SIGN, MAGNITUDE, VALIDITY of the channels, CHANNEL_FRAME, and SECOND_OF_TOT are clocked out by CHAN_CLK. MUX_CODE and ONE_BIT_SEL are unclocked inputs which for any particular mode are static.

MUX_CODE signals are decoded by the prom function defined in file MUXDCODE.MEM to produce signals MXC2 and MXC3. These control the counters which produce MUX_SEQ. For 1:1 mode the counters are held in reset; for 2:1 mode the counters are configured as 1 bit binary; for 4:1 mode the counters are configured as 2 bit binary. MUX_SEQ controls multiplexer functions which construct the channel signals from TRACK_DATA and VALID_IN. In one bit mode MAGNITUDES are forced to logic one. VALIDITY is the AND function of the individual validity signals for Sign and Magnitude.

T_REF_SOT is delayed and synchronised to produce SECOND_OF_TOT whose leading edge coincides with the leading edge of CHANNEL_FRAME. CHANNEL_FRAME is a delayed and resynchronised version of TRACK_FRAME modified by DDVCLK. DDVCLK is a signal which marks the bit position in the data and validity signals from where validity information was extracted. This bit position is now always logic zero. This ‘marker’ is inserted into the CHANNEL_FRAME signal. .

Waveform diagrams illustrating 4:1 multiplexing and 2:1 multiplexing are shown in Figure 3 and Figure 4.

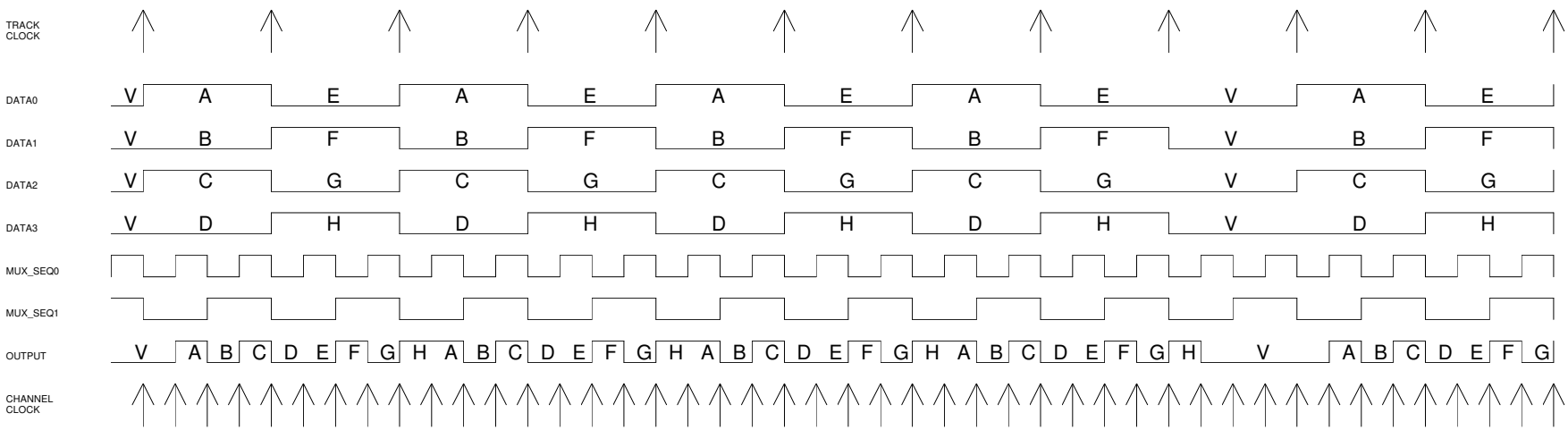

Figure 3. 4:1 MULTIPLEXING (pipeline delays not shown)

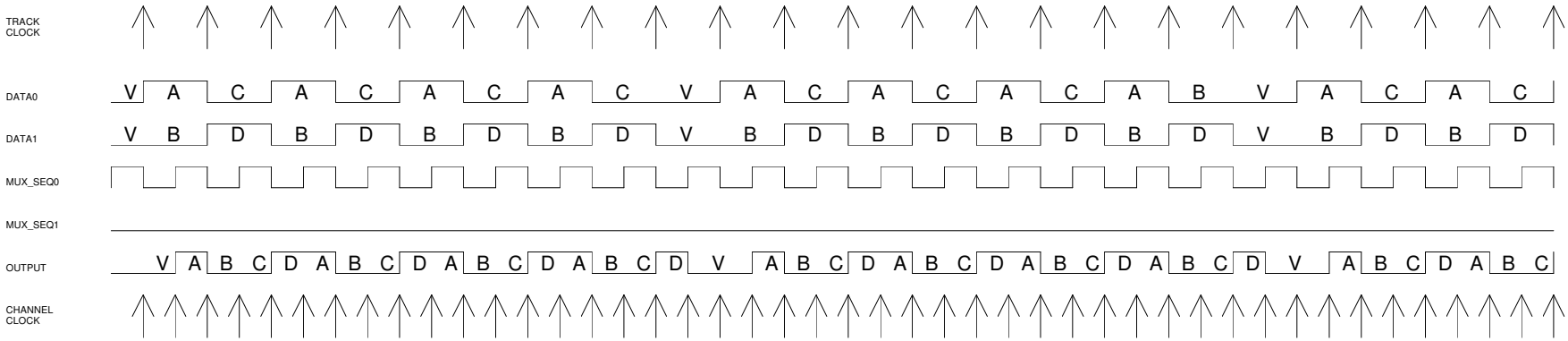

Figure 4. 2:1 MULTIPLEXING (pipeline delays not shown)

1664010010 (DMUX)

This FPGA implements the 1:2, and 1:4 de-multiplexing modes. That is one input track to two output channels, and one input track to four output channels. In these modes, Channel Clock frequency is always less than Track Clock frequency.
TRACK_DATA, VALID_IN, TRACK_FRAME, T_REF_SOT, and DDVCLK are clocked in by TRACK_CLOCK. All de-multiplexing clocking is by TRACK_CLOCK. SIGN, MAGNITUDE, VALIDITY of the channels, CHANNEL_FRAME, and SECOND_OF_TOT are synchronised to the lower frequency when clocked out by CHAN_CLK. MUX_CODE and ONE_BIT_SEL are unclocked inputs which for any particular mode are static.

MUX_CODE signals are decoded by the prom function defined in file MUXDCODE.MEM to produce signals MXC4 and MXC5. MXC4 is valid (logic one) for 1:4 de-multiplexing and MXC5 is valid (logic one) for 1:2 de-multiplexing. MXC5 is also the high order bit of DMUX_SEQ. The low order bits of DMUX_SEQ are a two bit binary count with a hold to extend the count to nine. This matches the nine bits in a byte and is synchronised to TRACK_FRAME and DDVCLK with appropriate delays such that the hold aligns with the bit position which originally was the validity bit. The validity bit position is sampled in the de-multiplexing circuitry every fourth byte, controlled by VT4, in both modes. The validity bit position is also sampled every second byte, controlled by VT2, in 1:2 mode only.

Each mode has a separate signal route through the de-multiplexing circuit. Which route is active is controlled by MXC4 and MXC5. De-multiplexing is achieved by sampling the signal at the appropriate time. DMB0, DMB1, DMB2, and DMB3 are four sampling control signals for 1:4 mode. These always sample the signal. In 1:2 mode additional sampling control signals CARRY0, CARRY1, BORROW2, and BORROW3 are generated. All sampling control signals are generated from DMUX_SEQ. A set of two or four sampled outputs have staggered delays from one output to the next. Extra delays are applied as appropriate to re-align the sampled outputs.

At this point the duration of each sample is not always four (1:4 mode) or two (1:2 mode) TRACK_CLOCK periods. A GATE signal is generated and synchronised to TRACK_FRAME with a mark to space ratio of 1:4 or 1:2 set according to the mode. This signal is used to regularise the sampled outputs which are then clocked out by CHAN_CLK.

Waveform diagrams illustrating 1:4 de-multiplexing and 1:2 de-multiplexing are shown in Figure 5 and Figure 6.

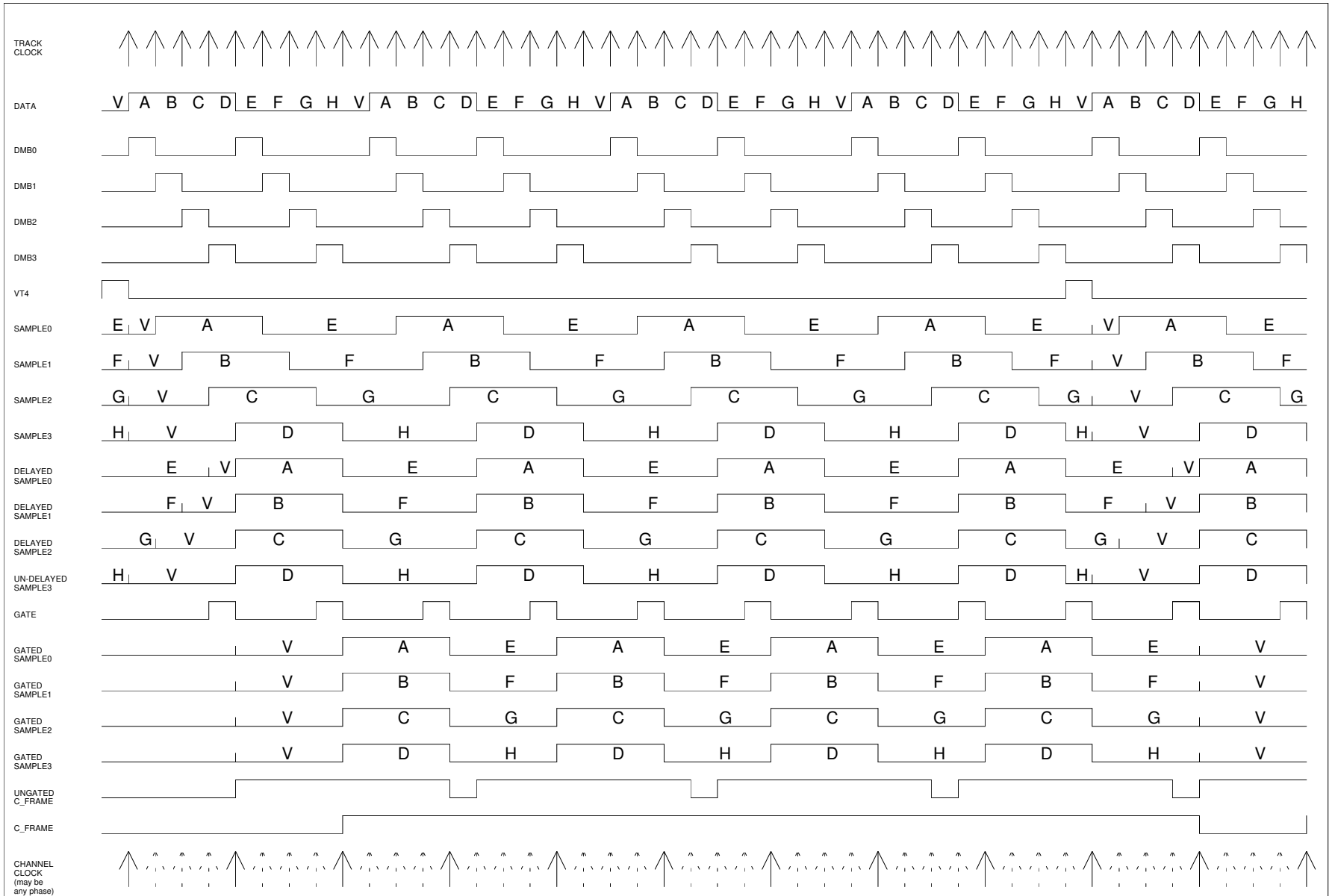

Figure 5. 1:4 DE-MULTIPLEXING (pipeline delays not shown)

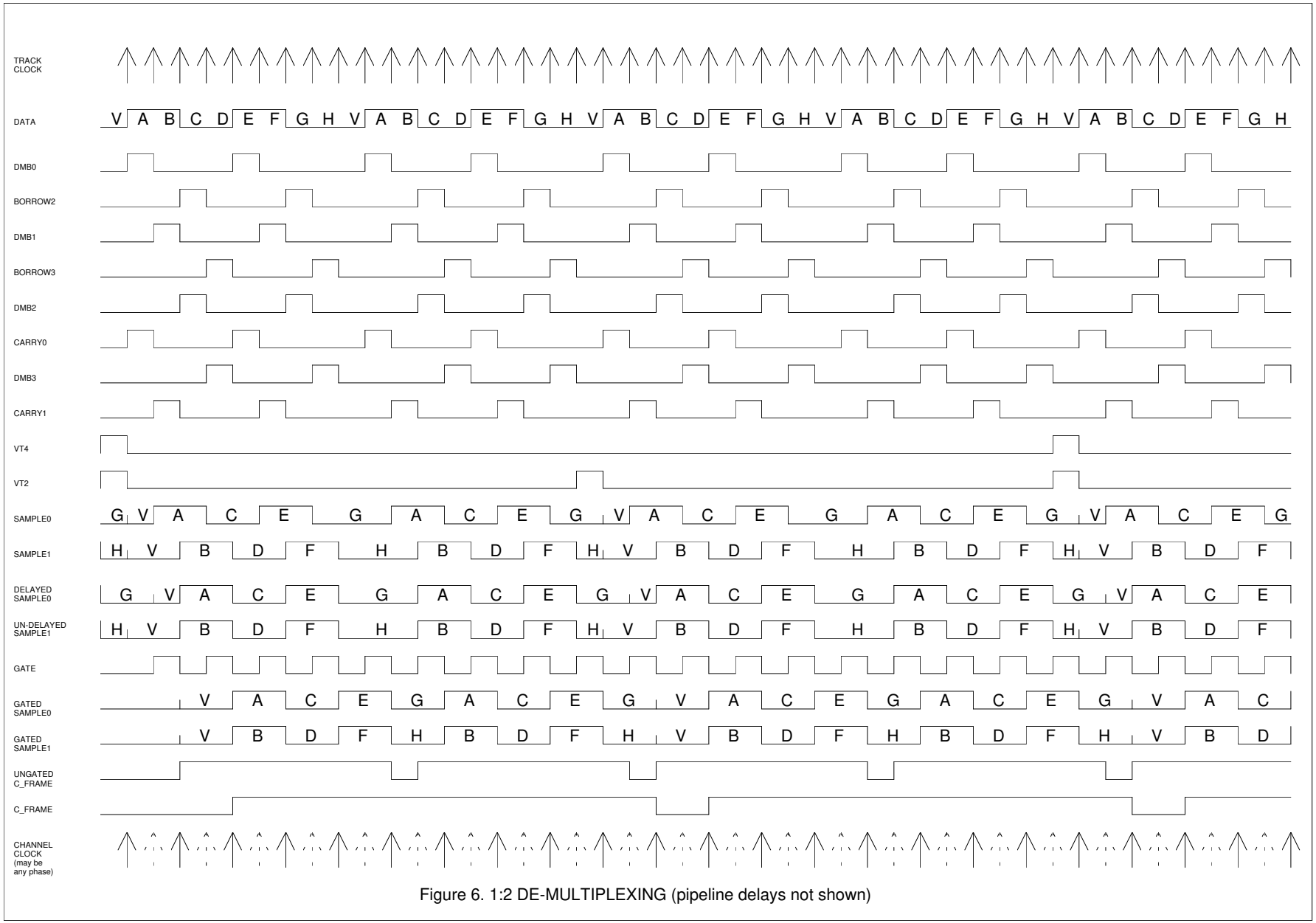

Figure 6. 1:2 DE-MULTIPLEXING (pipeline delays not shown)