Correlator meeting, Jonathan and Salvatore's room, September 5 2013, 11.00 am
Present: Jonathan, Salvatore, Des, Harro

agenda
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actions:
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topics:
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updates

aob

-updates

Jonathan mentioned the visit of Xilinx reps of last Friday and that it was a good one. However, the contents of the visit are probably more appropriate for discussion in Uniboard^2.

The DSPbuilder setup on Jonathan's machine is still not working, waiting for ICT to fix some things.

3 or 4 licenses are necessary: DSPbuilder (temporary - 30 days, Altera), Matlab (check), Simulink (named license was transferred from Salvatore => Jonathan) and a third party Matlab toolbox "fixed point toobox". The latter is necessary to run DSPbuilder but would probably also be useful for Uniboard firmware development; Matlab modelling could be done using fixed point arithmetic which makes analysis of the designs and the effect of different choices ("what if we drop one bit from this number ...") a lot easier.

This license is not available yet but maybe someone in ASTRON holds one so Jonathan & Salvator are going to ask the ASTRON firmware devs as well as ICT about it - the named Simulink license was transferred from an ASTRON person who wasn't using it anymore.

Des finished implementing the clock-offset code in all of the Erlang code (Harro thanks him) and is now busy testing the results.

Salvatore has started work on redesigning the packet_rx module to support receiving arbitrary sized VDIF frames.

Des + Harro discussed how to move on to make jive5ab send VDIF formatted data (so we could e.g. correlate directly from Mark5 disk packs). Most likely we're going to let jive5ab send the de-channelized and VDIF formatted data via a local TCP (or Unix) socket to the Erlang vdif_sender, which in turn will do the timing of the data and sending it to UniBoard. This is probably for now the fastest and easiest way to accomplish this.

- next meeting

Thursday 12th September 11.00 am, after jive coffee