UniBoard Correlator Startup

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Filter Configurations and Sub-band Allocation

Different channelizing filter configurations are supported by re-programming the front node FPGAs. The table shows the configurations available.

Firmware version	Input sub-bands	fbins per sb	Real time BW per sb	Sub-band to BN mapping	Config code
fn_4_1024	4	1024	16MHz	a(0-1023) → BN0 b(0-1023) → BN1 c(0-1023) → BN2 d(0-1023) → BN3	0x005b0a04

Erlang Drivers

Access to internal registers in the FPGAs is provided by three Erlang driver files:

> evn_tengbe.erl All ten gigabit interface registers in both front and back nodes
> evn_fn.erl   Front node registers
> evn_bn.erl   Back node registers

Ten GbE Port Initialization

After programming an FPGA the ten gigabit ports should be initialized with a valid MAC address and IP address. The Erlang command is:

```
uniboard:map(Board, fun evn_tengbe:init/6, [{NODE, PORT, MACADDR, IPADDR, GATEWAY, SUBNETMASK}]).
```

```
With parameters:
NODE = fn0, fn1, fn2, fn3, bn0, bn1, bn2 or bn3
PORT = 0 (currently only one 10GbE port per node)
MACADDR = MAC address in hexadecimal eg  16#00228608AA01
IPADDR = Local IP address in hexadecimal eg  16#C02A786a
GATEWAY = last octet of gateway address eg 16#69
SUBNETMASK = last octet of subnet mask eg 16#F8
```

Station Settings

Source

Each front node can receive data from eight stations. For each station there are a number of sub-bands (4 for version fn_4_1024). The stations and sub-bands are identified by a UDP port number which is hard coded into the firmware. The port numbers are allocated sequentially starting at 50000. Since the same UDP port numbers are re-used in every front node, a data channel is identified completely by its UDP IP address and port number.

Station	Band	Polarization	UDP Port no (decimal)
0	a	0	50000
0	a	1	50001
0	b	0	50002
0	b	1	50003
0	c	0	50004
0	c	1	50005
0	d	0	50006
0	d	1	50007
1	a	0	50008
1	a	1	50009
1	b	0	50010
1	b	1	50011
1	c	0	50012
1	c	1	50013
1	d	0	50014
1	d	1	50015
2	a	0	50016
2	a	1	50017
2	b	0	50018
2	b	1	50019
2	c	0	50020
2	c	1	50021
2	d	0	50022
2	d	1	50023
3	a	0	50024
3	a	1	50025
3	b	0	50026
3	b	1	50027
3	c	0	50028
3	c	1	50029
3	d	0	50030
3	d	1	50031
4	a	0	50032
4	a	1	50033
4	b	0	50034
4	b	1	50035
4	c	0	50036
4	c	1	50037
4	d	0	50038
4	d	1	50039
5	a	0	50040
5	a	1	50041
5	b	0	50042
5	b	1	50043

5	c	0	50044
5	c	1	50045
5	d	0	50046
5	d	1	50047
6	a	0	50048
6	a	1	50049
6	b	0	50050
6	b	1	50051
6	c	0	50052
6	c	1	50053
6	d	0	50054
6	d	1	50055
7	a	0	50056
7	a	1	50057
7	b	0	50058
7	b	1	50059
7	c	0	50060
7	c	1	50061
7	d	0	50062
7	d	1	50063

Station Attributes

Set station polarization and resolution in register 0x1

Single or dual polarization – *if we assume data is always 2 pol we don't need this*

resolution of input data

2 bit, 4 bit or 8 bit supported. Can add 1 bit if needed. May drop 4 bit if it is never used. Full implementation of 8 bit will require second DDR buffer and 10GbE port.

Integration Time

Set to an integer number of FFT periods in both the FN (register 0x0b) and the BN (register 0x00)

Process Batch Size

Set to an integer number of integration periods in the FN (register 0x02)

Buffer Segmentation

Set the number of segments in the input buffer the FN (register 0x4e). Default 4.

Normalization

Initially just set it in register 0xe. Use 0x14141414 for test data.

Later can use to monitor say once per second.

Product Selection

The product table in the back node determines which products are to be exported for post processing. To set up the product table, call the enable_product function with a list of products to enable as in the following example. All products not in the list will be skipped. The function sends the products and then toggles the ready bit to tell the firmware to convert the products into jumps.

```
uniboard:map(Board, fun evn_bn:enable_product/2,[{bn0, [16#07c0, 16#0600, 16#07d0, 16#0100]}]).
```

Start Processing
Read FN register 0x4d bit 0 to check if 'fifo' is full.
Send a nominal seconds worth of data and delay.
Write the batch size for the just written buffer segment to FN register 0x02 to indicate that processing can begin.

Error and Status

Firmware version

Component pio_firmware_version

Addr	R/W	VHDL name	Function
0x0	RO	c_firmware_version	32 bit version code

Version code to be incremented when firmware is modified. Codes 0x0000000-0x0000ffff reserved for test versions. Codes >= 0x00010000 reserved for production versions.

Firmware configuration

Component pio_firmware_config

Addr	R/W	VHDL name	Function
0x0	RO	c_firmware_config	32 bit configuration code
			bit 31 – 0 for FN (station based processing)
			1 for BN (correlator)

For a FN design bits 30:0 are defined as follows
    bit 7:0 – sub-bands per station
    bit 15:8 – FFT size (fbins = 2^FFT size)
    bit 21:16 – DDR size (local address width)
    bit 23:22 – number of DDR3 modules used
    bit 30:24 – configuration (000000 indicates 8 station, 2 filter bank architecture)
For a BN design bits 30:0 are defined as follows

General Status register
bit 31 = '1' indicates an error
Control system to read error regs once per second.
List of errors

List of Registers

1. Registers in module fn:pkt_rx

Addr	R/W	VHDL name	Function
0x00	RW	control	main control register
			bit 0 - active low soft reset to 10GbE and DDR
			bit 1 – toggle high to start test

			bit 2 – set '1' for real time, '0' for pre-recorded data
0x01	RW	data_attribs0	resolution, polarizations, station active for all 8 stations (see coding table)

        bit 0 – station 0 polarizations
        bit 1 – station 1 polarizations
        bit 2 – station 2 polarizations
        bit 3 – station 3 polarizations
        bit 4 – station 4 polarizations
        bit 5 – station 5 polarizations
        bit 6 – station 6 polarizations
        bit 7 – station 7 polarizations
        bits 9:8 – station 0 resolution
        bits 11:10 – station 1 resolution
        bits 13:12 – station 2 resolution
        bits 15:14 – station 3 resolution
        bits 17:16 – station 4 resolution
        bits 19:18 – station 5 resolution
        bits 21:20 – station 6 resolution
        bits 23:22 – station 7 resolution
        bit 31:24 – reserved

0x02	RW	numintegrations	bits 15:0 number of integrations to batch process (batch size)
0x0a	WO	start_second	TBD – time to start processing data
0x0b	RW	tintegrate_in_ffts	
0x0c	RW	data_attribs1	VDIF framelength. Defaults to 0x00000275. Do not change.
0x0e	RW	normalize	Normalization codes for four filter banks

        bits 4:0 – filterbank 0
        bits 12:8 – filterbank 0
        bits 20:16 – filterbank 0
        bits 28:24 – filterbank 0

0x10	RO	diag0	Main status register

        bit 0 – DDR init done ('1' indicates DDR controller initialized)
        bit 1 – DDR ready ('1' indicates DDR ready for access)
        bit 2 – all fn ready ('1' indicates all four Fns synchronized)
        bit 31 – error ('1' indicates an error in the error register)

0x11	RO	diag1	Diagnostic information

        bits 15:0 – Station code of last received VDIF frame
        bits 31:16 – low 16 bits of last received VDIF frame number

0x12	RO	diag2	Diagnostic information

        bits 9:0 – Thread ID of last received VDIF frame

0x13	RO	diag3	Diagnostic information

        bits 23:0 – Framelength of last received VDIF frame

0x14	RO	diag4	Diagnostic information

        bits 31:0 – Time in seconds from last received VDIF frame

0x15	RO	diag5	Diagnostic information

        bits 26:0 – Current DDR local address

0x16	RO	diag6	Diagnostic information

        bits 31:0 – FFT period count within integration

0x17	RO	diag7	Diagnostic information

        bit 0 – '1' indicates data processing has started
        bit 1 – readfifo status for filterbanks 0 & 1
        bit 2 – readfifo status for filterbanks 2 & 3

			bits 10:8 – status of startup state machine
0x1d	RO	dummy_register0	To be removed in production version
0x1e	RO	dummy_register1	To be removed in production version
0x20	RO	framecount(0)	Clear-on-read count of frames for station 0, band 0
0x21	RO	framecount(1)	Clear-on-read count of frames for station 0, band 1
0x22	RO	framecount(2)	Clear-on-read count of frames for station 0, band 2
0x23	RO	framecount(3)	Clear-on-read count of frames for station 0, band 3
0x24	RO	framecount(4)	Clear-on-read count of frames for station 1, band 0
0x25	RO	framecount(5)	Clear-on-read count of frames for station 1, band 1
0x26	RO	framecount(6)	Clear-on-read count of frames for station 1, band 2
0x27	RO	framecount(7)	Clear-on-read count of frames for station 1, band 3
0x28	RO	framecount(8)	Clear-on-read count of frames for station 2, band 0
0x29	RO	framecount(9)	Clear-on-read count of frames for station 2, band 1
0x2a	RO	framecount(10)	Clear-on-read count of frames for station 2, band 2
0x2b	RO	framecount(11)	Clear-on-read count of frames for station 2, band 3
0x2c	RO	framecount(12)	Clear-on-read count of frames for station 3, band 0
0x2d	RO	framecount(13)	Clear-on-read count of frames for station 3, band 1
0x2e	RO	framecount(14)	Clear-on-read count of frames for station 3, band 2
0x2f	RO	framecount(15)	Clear-on-read count of frames for station 3, band 3
0x30	RO	framecount(16)	Clear-on-read count of frames for station 4, band 0
0x31	RO	framecount(17)	Clear-on-read count of frames for station 4, band 1
0x32	RO	framecount(18)	Clear-on-read count of frames for station 4, band 2
0x33	RO	framecount(19)	Clear-on-read count of frames for station 4, band 3
0x34	RO	framecount(20)	Clear-on-read count of frames for station 5, band 0
0x35	RO	framecount(21)	Clear-on-read count of frames for station 5, band 1
0x36	RO	framecount(22)	Clear-on-read count of frames for station 5, band 2
0x37	RO	framecount(23)	Clear-on-read count of frames for station 5, band 3
0x38	RO	framecount(24)	Clear-on-read count of frames for station 6, band 0
0x39	RO	framecount(25)	Clear-on-read count of frames for station 6, band 1
0x3a	RO	framecount(26)	Clear-on-read count of frames for station 6, band 2
0x3b	RO	framecount(27)	Clear-on-read count of frames for station 6, band 3
0x3c	RO	framecount(28)	Clear-on-read count of frames for station 7, band 0
0x3d	RO	framecount(29)	Clear-on-read count of frames for station 7, band 1
0x3e	RO	framecount(30)	Clear-on-read count of frames for station 7, band 2
0x3f	RO	framecount(31)	Clear-on-read count of frames for station 7, band 3
0x4d	RO	synchronizationfifo_full	bit 0 full signal from synchronization fifo
0x4e	RW	synchronizationfifo_max	bits 7:0 number of segments in the buffer
0xfe	RO	framecount_nomatch	Clear-on-read count of frames which did not match a station/thread
0xff	RO	error_register0	To be determined

data_attribs0 binary coding
Polarizations
'0' – station is single polarization
'1' – station is dual polarization (both polarizations packed into a single VDIF frame)

Resolution
00 – station is 1 bit sample resolution (not currently implemented)
01 – station is 2 bit sample resolution

10 – station is 4 bit sample resolution
11 – station is 8 bit sample resolution

2. Registers in bn:corner_turner

Addr	R/W	VHDL name	Function
0x0	RW	control	main control register bit 0 - active low soft reset to 10GbE and DDR bit 1 – toggle high to process next freq bin in single step mode bit 2 – toggle high to start a new integration in single step mode bits 27:16 – set integration period in single step mode
0x1	RO	diag0	Diagnostic information bit 0 – DDR0 init done ('1' indicates DDR controller 0 initial'd) bit 1 – DDR1 init done ('1' indicates DDR controller 1 initial'd) bit 2 – '1' indicates write to DDR0, read from DDR1 '0' indicates write to DDR1, read from DDR0 bit 30 – '1' indicates data received from Fns bit 31 – '1' indicates integration in progress
0x2	RO	diag1	Diagnostic information bit 31:0 – Sync status of mesh transceivers
0x3	RO	diag2	Diagnostic information bit 31:0 – FFT period within integration received from FN
0x4	RO	diag3	Diagnostic information bit 31:0 – Integer seconds part of time stamp of integration period received from FN
0x5	RO	diag4	Diagnostic information bit 26:0 – Current DDR write address
0x6	RO	diag5	Diagnostic information bit 26:0 – Current DDR read address
0x7	RO	diag6	Diagnostic information bit 9:0 – Last frequency bin processed

3. Registers in the bn product table

Addr	R/W	VHDL name	Function
0x000-0x83f	WO	u_ctrl_mem	Each address controls one product (see product table) bit 0 – '0' to skip corresponding product bit 0 - '1' to send corresponding product
0x840-0xfff	WO		Not used

4. Register in the bn product table ready

Addr	R/W	VHDL name	Function
0x0	WO	ready	toggle high to convert the product table to jumps