UniBoard correlator implementation and control meeting
Minnaert Room, Thursday February 4, 2010

present: Jonathan, Ying, Ronald, Arpad, Harro, Des, Paul

agenda

- test firmware, status and timeline
- correlator firmware
- control software, NIOS operating system

Jonathan: design bn_ddr (item 2 in list of test firmware) compiles and simulates without errors. This now needs to be checked and possibly expanded to a more rigourous test (Items 11 and 12).

Design fn_allinfra which incorperates all the interfaces compiles with a timing error
on the slow JTAG clock which seems to be an Altera bug.

Jonathan is simulating software to test the configuration PROM (Item 4)
Ying is working on the interface between the Nios and the Ethernet port, which it seems clear should
include state machines to assemble and dissassemble the UDP headers
Harro is looking at the OSes.

Harro: problematic to make Altera muRTOS small enough, have to include lots of functionality which is not needed. freeRTOS is much more bare boned, looks like solution will be to do simple interrupt handling and reading and writing of FPGA memory, no IP stack needed.

Eric and Daniel are starting on item 6, adapting the Lofar firmware to test the FN-BN mesh.

Jonathan has compiled the Lofar filter bank with 4096 points and various window lengths
to look at resources. Need to simulate it next.