JUC meeting, August 21 2013, Arpad's room

present: Jonathan, Harro, Des, Arpad

Jonathan: working with Harro on 2-pol bug. L par ok, R par mangled. Turns out to be a pipeline error, products are calculated ok, but real part is picked up from wrong pol. The same problem may affect multiple station operation as well. Being worked on, solution not simple.

Clock offsets: Jonathan to check in the code with the new registers so that Des can use them.

The correction will be applied before the DDR, at VDIF frame resolution (time and frame nr). Finer correction in delay model.

Harro still needs to change VDIF reader for this. Next week, after 2pol bug fixed, attempt clock offset, multiple stations.