Correlator Implementation and Control meeting, November 1 2012, Arpad's room

present Jonathan, Salvatore, Harro, Des, Arpad

action items

Jonathan: test fix of Erlang performance problems reading UDP packets (on hold)
Jonathan + Salvatore: figure out how to make packet spacing adjustable (on hold)
Harro: save N11L4 scan 11 reference data to LTO4
#done remove
Jonathan: inform Des when buffer addressing documentation is updated
done remove
Harro: create more N11L4 VDIF data
not done
Harro: talk to Mike Sipior re casa
done, but no clear solution. Mike is not in charge of case anymore. Only Glish is being used by dr. Bob, nobody wants to start programming in glish. There must be other pyton-based plotting packages, and
casa/casacore surely must run on some linux machines. ***action*** Harro to talk to Ger

updates

Jonathan: a certain amount of pressure is felt downstairs, getting data in but
mangled data out. Output FN seems fine, signal tap in BN between corner turning and validity accumulator. Will make test bench with only corner turner simulation to save time, whole BV takes 5 hours. Maybe fault in cornerturning. Used to do single integration, now continuous, used to do 2 stations, now 8. Maybe memory mapping wrong.

Discussion about long times for simulation. Dop233 currently not used, because it is not easy to copy complete development environment. Not needed, should be possible to mount home disks from dop233, using sshfs (NSF no good, different domains). ***Action Harro***
New PCs not really a solution, as they have more cores but most tools are single threaded anyway.

Des: could use design anyway to start testing getting data into UB,

even if output is rubbish. Harro: need more VDIF data? Answer yes.

Salvatore: is it possible to run everything on Unictl. Harro: yes, possible, use a node on Unictl to talk to FPGA. Has old Ubuntu, old Erlang. **action Harro** send ticket to Paul.

Jonathan: 10G from UB to what? AriBox most obvious, ***action Harro** ask Paul if AriBox reachable.