JUC meeting, August 1, 2013, 11.00 am, Arpads room

present Jonathan, Salvatore, Arpad

Salvatore is working on re-write of packetRX, with help from Jonathan. Writing to DDR (without actual DDR interface) seems to be sorted, work on reading now ongoing. Design has changed from easy writing--complicated reading, to complicated writing--easy reading. When this is done, the validity will be done, then the control. Validity will be stored as one bit per frame, in a mirror-FPGA memory. Still need to check if enough memory is available.***action

Jonathan is working on the statistics module, now using Megawizard to ensure real memory gets created. Wonders about stats, whether it should be calculated once per integration, or every few integrations, but continuously, or continuously. Need to talk to Mark about SFXC practice. ***action Jon

Jonathat: 2nd pol does not mess up 1st pol, but not checked with real data. Should be done. More stations: waiting for Des to return, issues with control code. No clock offset yet applied, should be done, even though this will have to go into new packetRX, needs to be implemented now. Then, more stations.