Minutes from the meeting of: Thursday May 24th.
Present: Jonathan, Salvatore, Des, Harro

Action items of last meeting

Jonathan: publishing documents on the wiki is underway, awaiting account details

Jonathan/Salvatore: working on MATLAB code to interpret the packet header so
implementing putting the 8-bit FPGA node-id and - left to Jonathan/ Salvatore
to decide how many bits wide - correlation engine id in the packet header will happen on a short timescale

Jonathan: MATLAB seems to support client/server operation via sockets. Des and Harro suggest that the Erlang datacapturer can be persuaded to send the captured data immediately over the network rather than going through a file-write and read mechanism

Individual updates

Jonathan/Salvatore: the gatelevel simulation ran last week was very succesfull in pinpointing the place where a timing error on a multi-cycle path happened. The component was fixed and tests with noise-free sinusoidal data and using signal taps before and after the component indicate the issue
is now fixed. The data goes through the filterbank ok now. There are less known bugs.

Changes in the backnode triggered the receiver to sometimes loose synchronization. This is under investigation.

Jonathan did set up the erlang model coefficient sender but must first un-hardcode the model coefficients in the VHDL.

Des: it looks like having one (1) second of delay makes the quadratic coefficient almost creep up into the 8th bit behind the decimal point in the proposed 24.8 fixed point delay coefficient format. Jonathan mentions that only 4 bits of precision are actually used, so the format might change to 28.4 fixed point. Will discuss offline. It becomes obvious that supporting space-based VLBI has a big effect on the model coefficients and precision. We should find out exactly how much we have to/want to support space VLBI.

Harro: started to generate/parse JSON metadata files for interpreting Bob's data and building (internal) datastructures.

Action items

Jonathan/Salvatore: update output data packet header with 8-bit FPGA node-id

and possible >1 bit correlation engine id. Update documentation and put on the memoseries wiki

Des: request worst space based acceleration values from Dmitry

Harro: contact Arpad to inquire what we promised the EC we would support in the space VLBI department

Next meeting

Harro is absent through Thursday next week so it was agreed to meet again on Friday June 1st, somewhat after coffee