VLBI test observations with 8bit quantization data

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1. VDIF data with 8-bit quantization

VDIF: VLBI Data Interchange Format

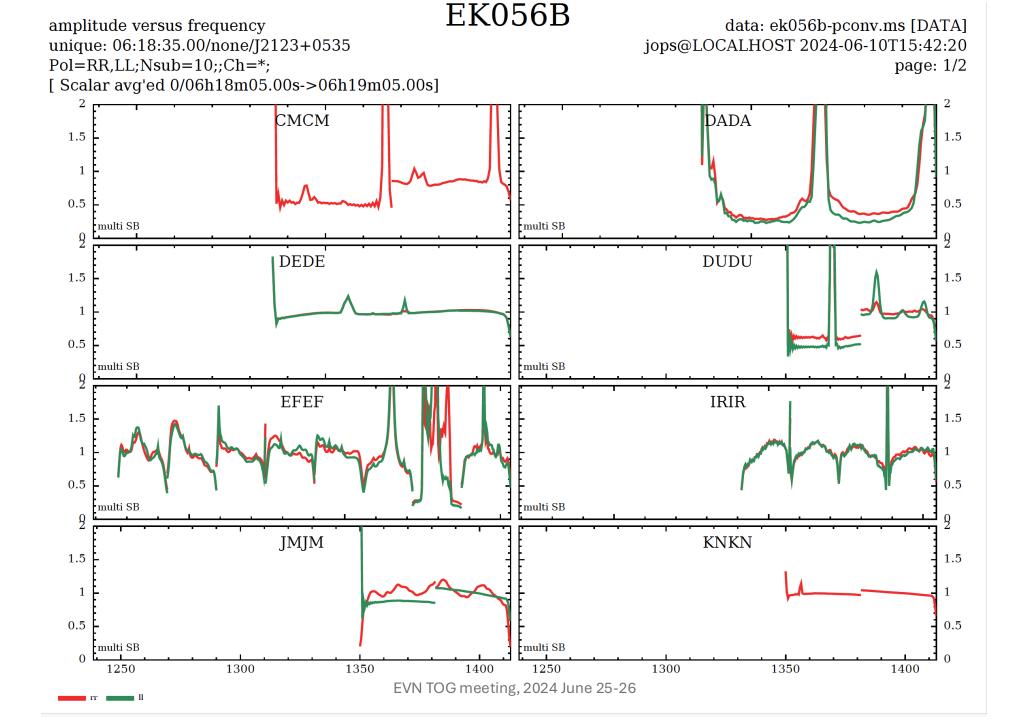
Advantages

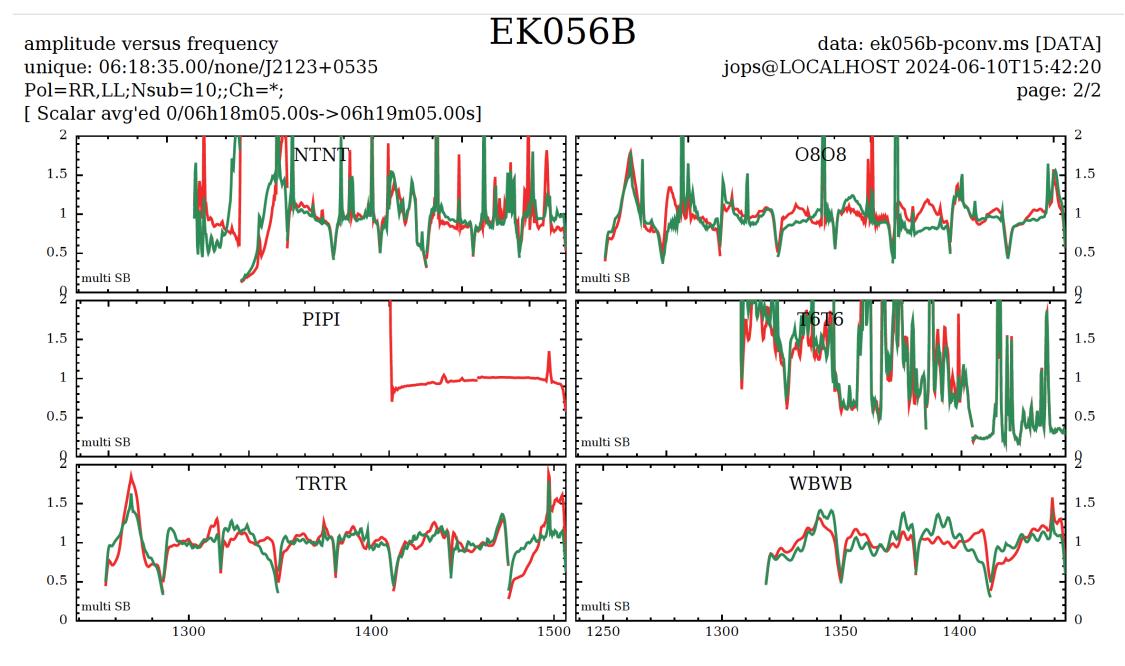
 Theoretically, improve the quantization efficiency from 88 % (2 bits/4 levels) to 100% (8 bits/256 levels).

 \circ Increase system linearity and reliability in case of strong and varying RFIs.

- More stable correlation amplitude on short timescales of <~10 sec.
- More stable bandpass shapes during the observations.
- Disadvantages

 \odot Require more disk space, a factor of four higher.





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2. Potential applications

- Future 4-Gbps e-VLBI observations at L band
 - \circ No need to buy more disks.
 - Hard to effectively increase bandwidth at L band because of RFI.
 - Image sensitivity improvement => one more 30-m dish for the EVN
 - 10% in case of no RFI.
 - >10% in case of strong RFI.
- Narrow-band spectral line VLBI observations.
- FRB monitoring observations with VLBI backends. o 500-1000 hours per year at On, Tr, Wb, Ir et al.
- Simple option for stations to improve sensitivity at L band with more disks during the EVN sessions.
- Future SKA-VLBI observations at L band
 - $\,\circ\,$ 16 Gbps with ~512 MHz bandwidth at some stations: SKA-Mid, GMRT, FAST, Ef, On,...

3. Test observations with DDC E v126

- Backend: 2L2H DBBC3 with the firmware DDC E v126
- Experiment: PR327A (PRECISE project)
- Frequency setup for DBBC2 and DBBC3 at Onsala • Frequency: 1254-1510 MHz.
 - \circ Dual polarization.
 - $\odot\,\text{Data}$ rate
 - DBBC2
 - 2048 Mbps (2 bits, 32 MHz x 8, 1 VDIF thread), LO=708 MHz.
 - DBBC3
 - 8096 Mbps (8 bits, 128 MHz x 4, 2 VDIF threads) , LO=0 MHz.

- Schedule VEX file with NRAO Sched
 - \circ O8: DBBC2 backend.
 - \odot ON: DBBC3 backend.
 - \odot 2 bits for O8 and ON.
- Observation PRC and SNP files
 - \odot SNP file from FS Drudg.
 - PRC file from FS Drudg and hands-on editing.
 - core3h01=\$

- => <mark>core3h01</mark>
- fb_mode=vdif,,,256.0
- => fb=mode=vdif_8000-8192-4-8
- Adding the procedure sched_initi in the experimental PRC file
- Inserting DBBC3 commands dbbc8bit in the procedure sched_initi
- Recording with JIVE5ab 3.1.0

 \odot Just do it. No special requirements.

- 2024.115.19:48:27.22&setup01/fb=mode=vdif_8000-8192-4-8
- 2024.115.19:48:27.22&setup01/fb_mode
- .
- 2024.115.19:48:36.83/fb/!mode=0;
- 2024.115.19:48:36.83/fb_mode/vdif_8000-8192-4-8,,,,VDIF,32,256.,8000

```
dbbc3=dbbc8bit=on,1,u,1
!+1s
dbbc3=dbbc8bit=on,5,u,1
!+1s
dbbc3=dbbc8bit=on,9,u,1
!+1s
dbbc3=dbbc8bit=on,13,u,1
!+1s
```

- Available DiFX tools to check the 8-bit VDIF data
 - Print VDIF header: printVDIFheader
 - Check sample RMS and Mean m5bstate
 - Find the starting time: m5time
 - Make auto-corrlation spectra: m5spec
 - Sometimes, catched many warning messages of "VDIF Validate ..." due to a tiny time offset.
 - In the program format_vdif.c, we changed the threshold from 0.000001 to 0.5 ns at Onsala.
 if(mjd_t != mjd_d || sec_t != sec_d || fabs((double)ns_t ns_d) > 0.000001)

 fprintf(m5stdout, "VDIF validate[%IId]: %d %d %f : %d %d %lld\n", ms->framenum, mjd_d, sec_d, ns_d, mjd_t, sec_t, ns_t);

return 0;

- Correlation at JIVE
 - o VEX 2.0 file: Provided by JIVE Python Sched and tiny hands-on editing.
 - thread = &DS0: &thread0 : 0 : 2 : 256 Ms/sec : 8 : real : 8000; thread = &DS1: &thread1 : 1 : 2 : 256 Ms/sec : 8 : real : 8000;

 $_{\odot}$ An upgrade of SFXC was implemented by Aard Keimpema.

• VDIF data format

 The output 8-bit VDIF data from DDC E v126 follows the format of two's complement instead of offset binary.

• <u>Fringe-test results</u> of 60-s scan No.123

• Stations: Ef, Mc and Onsala.

Webpage: https://services.jive.nl/ftp_fringes/PR327A/scan123/index.html

Bright fringes to DBBC3 (On) and DBBC2 (O8)

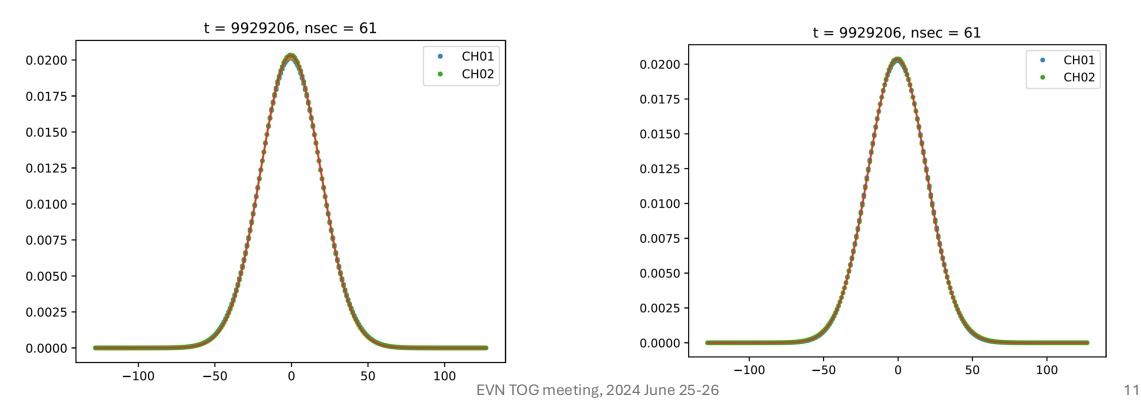
<u>Vex file</u> -- Scan name = No0123, total averaging time = 60.0 sec Timerange: 2024-04-24 22:06:46-22:07:46

pr327a	Auto correlations (BBC number)				Cross correlations (SNR, lag offset)							
	Ef	Mc	08	On	Ef-Mc	Ef-O8	Ef-On	Mc-O8	Mc-On	O8-On		
1286.00MHz, LSB, RCP-RCP	1		1	1		170101 M	<u>165.0AP</u> offset: 0			<u>65925.8AP</u> offset: 0	$ 1/1/1/00MH_{\alpha} $ I CD DCD DCD $ 2 $ $ 1 $ $ 2 $ $ 5 $	42.0AP 326.7AP 66.7AP 45.2AP 62232.52 offset: 1 offset: 0 offset: 0 offset: 0 offset: 0
1286.00MHz, LSB, RCP-LCP	Cross	hands				13.2AP offset: 0	<u>12.3AP</u> offset: -1			10643.3AP offset: -4		5.5AP ffset: 012.1AP offset: 05.2AP offset: 06.6AP offset: 08789.0A offset: 0
1286.00MHz, LSB, LCP-LCP	2		2	9			230.6AP offset: -1			88773.8AP offset: 0	$141400MH_{7}$ I SP I CP I CP 111 0 111 12	78.7AP 303.5AP 63.9AP 73.0AP 86733.3A offset: 0 offset: -1 offset: 0 offset: 0 offset: 0
1286.00MHz, LSB, LCP-RCP	Cross	hands				8.9AP offset: 1	8.9AP offset: 0			9250.1AP offset: 3		9.3AP20.9AP3.9AP5.0AP6623.2Aoffset: 1offset: 0offset: 13offset: -52offset: 0
1286.00MHz, USB, RCP-RCP	1		1	1		<u>204.1AP</u> offset: 0	<u>199.4AP</u> offset: -1			96361.1AP offset: 0	$141400MH_2$ USB PCP-PCP 3 2 3 5	48.8AP 216.1AP 53.4AP 59.5AP 63226.44 offset: 0 offset: -1 offset: 0 offset: 0 offset: -1
1286.00MHz, USB, RCP-LCP	Cross	hands				7.6AP offset: 0	<u>10.7AP</u> offset: 0			41925.6AP offset: 20		.2AP6.5AP4.7AP5.1AP5938.7Aoffset:12offset:-12offset:4
1286.00MHz, USB, LCP-LCP	9		9	9			208.9AP offset: 0			95918.6AP offset: 0	$141400MH_{7}$ USP I CD I CD 11 10 111 12	00.5AP 201.8AP 55.5AP 58.6AP 81093.3/ ffset: 1 offset: 0 offset: 0 offset: 0 offset: 0
1286.00MHz, USB, LCP-RCP	Cross	hands				<u>19.1AP</u> offset: 0				43516.3AP offset: -17	11/11/ OOMHZ LISB LCD DCD Cross hands	3.6AP ffset: 120.7AP offset: 04.8AP offset: 94.9AP offset: -635845.0A offset: -
1350.00MHz, LSB, RCP-RCP	2		2	1		218.7AP offset: 1	218.6AP offset: 1			<u>61203.1AP</u> offset: -1	$11/79 \text{ ANMU}_7 \text{ I SP DCD DCD} 1 2 1 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5$	30.4AP 123.5AP 18.7AP 13.6AP 81730.3/ ffset: 0 offset: 1 offset: 0 offset: 0 offset: 0
1350.00MHz, LSB, RCP-LCP	Cross	hands				<u>13.4AP</u> offset: 1	<u>14.9AP</u> offset: 0			9890.6AP offset: 0	11478 AAMUZ ISB BCDICDICross hands	<u>5.5AP</u> <u>5.5AP</u> <u>4.3AP</u> <u>4.9AP</u> <u>4855.7A</u> ffset: 0 offset: 39 offset: -57 offset: -51 offset: 0
1350.00MHz, LSB, LCP-LCP	<u>10</u>		<u>10</u>	9			203.2AP offset: 0			57127.8AP offset: 1	11/78 from 128 from 12 from	19.6AP 118.8AP 15.9AP 14.3AP 52197.3/ ffset: 0 offset: 0 offset: 0 offset: 1
1350.00MHz, LSB, LCP-RCP	Cross	hands				22.9AP offset: 0	<u>12.7AP</u> offset: 1			10704.8AP offset: 0		4.6AP ffset: 14.9AP offset: -54.4AP offset: 683.7AP offset: 653313.7A offset: 1
1350.00MHz, USB, RCP-RCP	2	1	2	1	<u>336.4AP</u> offset: 0	<u>340.0AP</u> offset: 0		<u>49.1AP</u> offset: 0	<u>46.3AP</u> offset: 0	<u>57770.6AP</u> offset: -1	1478.00MHz, USB, RCP-RCP 4 4 5	65.5AP 120.2AP 41536.7/ ffset: 0 offset: -1 offset: 0
1350.00MHz, USB, RCP-LCP	Cross	hands				9.8AP offset: -1		<u>4.0AP</u> offset: -35	<u>3.6AP</u> offset: 64	8586.9AP offset: -1	11478 00MHz USB RCP-LCPICross hands	3.4AP 13.1AP 5424.1A offset: 1 offset: 0 offset: 0
1350.00MHz, USB, LCP-LCP	<u>10</u>	9	<u>10</u>	9	2 <u>13.3AP</u> offset: 1	<u>347.6AP</u> offset: 0	<u>341.2AP</u> offset: 0	<u>40.6AP</u> offset: -1	<u>40.7AP</u> offset: 0	59058.3AP offset: 1		29.8AP 161.0AP 43556.02 offset: 1 offset: 0
1350.00MHz, USB, LCP-RCP	Cross	hands				24.0AP offset: -1		4.5AP offset: 28	3.6AP offset: 46	<mark>8453 7AP</mark> offset: 1	UI M/IN MANA Hay I HSR/ TO E PLOY CORE hands	8.7AP offset: 021.4AP offset: 1106244.1A offset: 0

• Sample distribution

IF AGC target value: 18000 instead of 35000 (for 0.5 GHz input signal).
 BBC AGC target value (power): 24000 (sample RMS ~6 from m5bstate).
 Switching off 80 Hz Cont-Cal signal, IF and BBC and AGC during scans.
 Following Gaussian distribution in the range of –127 to +127

- Voltage sample Mean ~0.1 and RMS ~20.
- Consistent with DiFX m5bstate output since it has a scale factor (3.3).

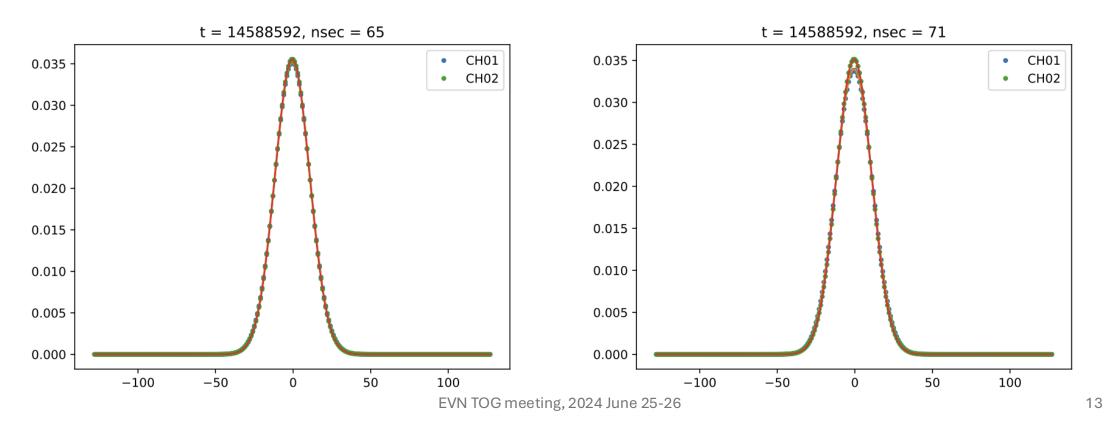


4. Test observations with DDC E&U v127

- Firmware changes: outputs <u>the standard VDIF data</u>, i.e. offset binary format.

 It begins with all 0's for the most-negative sampled value to all 1's for the most-positive sampled value. For example, 2 bit/sample coding is (in order from most negative to most positive) 00, 01, 10, 11, and nominal unpack values might be 3.336, -1, 1, 3.336.
- Experiment: <a>PR335A (PRECISE project)
- Frequency setup for DBBC2 and DBBC3 at Onsala
 - Frequency: 1254-1510 MHz.
 - o Dual polarization.
 - o Data rate
 - 08: DBBC2
 - 2048 Mbps (2 bits, 32 MHz x 8, 1 VDIF thread), LO=708 MHz.
 - ON: DBBC3 DDC E v127 in the 1st part
 - 8096 Mbps (8 bits, 128 MHz x 4, 2 VDIF threads) , LO=0 MHz.
 - ON: DBBC3 DDC U v127 in the 2nd part
 - 8096 Mbps (8 bits, 64 MHz x 8, 4 VDIF threads) , LO=0 MHz.
- Correlation results: https://services.jive.eu/ftp_fringes/PR335/index.html

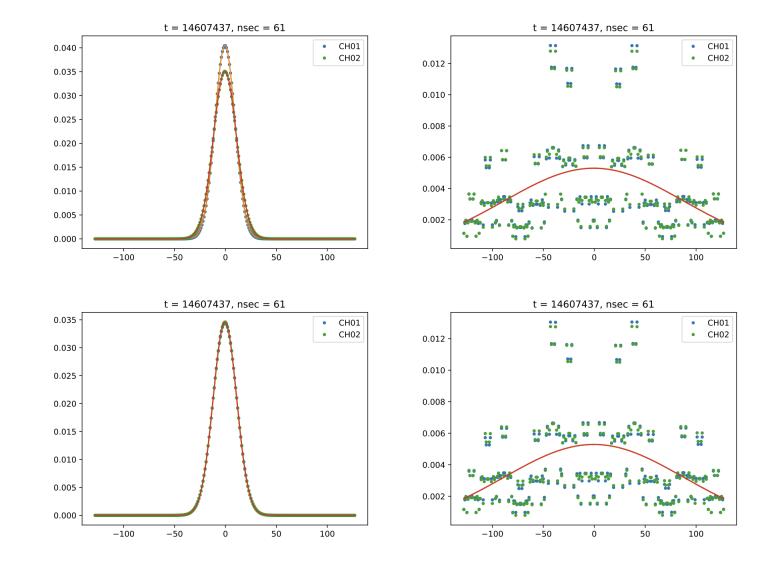
- Fringes to both DBBC2 and DBBC3 with comparable SNR!
- DDC E v127
 - $\circ~$ Calibrator scan: No. 24
 - $\,\circ\,$ Sample distribution between -127 and +127
 - BBC AGC target level: 8000.
 - Following Gaussian distribution: RMS ~11.5 (~3.5 from m5bstate), Mean ~0.
 - Fringes were seen in all 128 MHz subbands.



• DDC U v127

- $\circ~$ Calibrator scan: No. 111
- \circ BBC AGC target level: 8000
- Sample distribution in the lower two 64 MHz subbands
 - Following Gaussian distribution
 - RMS~11.5
 - Mean ~0
 - High-SNR fringes
- Sample distribution in the upper two 64 MHz subbands
 - 8-bit header, 2-bit meta data
 - Strange distribution.
 - A bug in the control software.
 - Fixed rapidly by Sven Dornbusch.

8-bit mode: Support 4 x 128 MHz filters per Core3H board



5. Summary and outlook

- VLBI test observations with 8-bit VDIF data went successfully

 DBBC3 backends do output sensible 8-bit VDIF data, in particular using
 the new firmware DDC E/U v127.
 - $_{\odot}$ The upgraded SFXC fully supports the correlation of 8-bit VDIF data.
- Follow-up thoughts
 - \circ A few more test observations with DDC E/U v127.
 - Justify 10% sensitivity improvement with more stations and careful setups.

- Required supports for future hands-off observations
 NRAO Sched
 - Tiny change: adding the option of 8 bit VDIF data format.

 $\circ \, \text{FS}$

- Drudg
 - Supporting VEX 2.0
- SNAP commands
 - core3h_mode
 - fb_mode

 $_{\odot}$ JIVE5ab and SFXC

- Done?
- \circ DBBC3 firmware DDC
 - Improve the bandpass shape of 32 MHz filters
 - Minimize bandpass mismatch on the baselines of DBBC3-DBBC2 .
- Thank Gino and Sven for helpful email discussion!