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TO: Mark 5B Development Group
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SUBJECT: Mark 5B DIM parameters and procedures

Below is an updated list of the DIM parameters with expanded descriptions, plus a simple scenario of the sequence of actions required to setup and use the DIM in practice, plus suggested procedures for managing interrupts. **Updates from previous version are in red.**

Read/write parameters:

Word	Bit(s)	Name	Description
0	13	REQ_II	0 – DIM will operate in FPDP mode 1 – DIM requests to operate in FPDP-II mode (subsequent reading of Word E, bit 13 is required to determine whether everyone on the bus agrees to this request)
	12	SELDOT	1 – Enable DOT1PPS as PCI interrupt source
	11	SELDIM	1 – Enable external 1PPS (as chosen by SELPP) as PCI interrupt source
	10	TVGSEL	0 – Select external sample data as DIM input data 1 – Select tvg as DIM input data
	9	SELTVCNT	0 – tvg will create VSI tvg pattern 1 – tvg will create 32-bit incrementing pattern, starting at zero on start of scan and resetting to 0x00000000 every 100 seconds thereafter. Note: tvg will be driven by clock signal selected by SELCGCLK.
	8-6	K	Specifies input clock frequency: $f_{\text{CLOCK}}=2^{(k+1)}\text{MHz}$, $0 \leq k \leq 5$
	5-3	J	Decimation parameter for input sampling: decimation ratio= 2^j , $0 \leq j \leq 4$, $j \leq k$
	2-1	SELPP	Select external 1PPS source: 0 – No 1PPS selected 1 – ALTA1PPS 2 – ALTB1PPS 3 – VSI1PPS
	0	SELCGCLK	Select source of input clock: 0 – VSI clock 1 – Clock generator
1	15-14	LED7	Control LED #7 according to the following code: 00 – off; 01 – red; 10 – green; 11 – blue
	13-12	LED6	Control LED #6 according to the following code:

			00 – off; 01 – red; 10 – green; 11 – blue
	11	DIM_CASC	1 – enable input VSI bit streams to appear at the VSI output ('cascade')
	10	EN_VSI_OUT	1 – enable VSI output drivers
	5	1_BIT_S	0 – 2 bit/sample assumed by phase-cal extractor 1 – 1 bit/sample assumed by phase-cal extractor
	4	PC_INT_EN	0 – disable phase-cal interrupts 1 – enable phase-cal interrupts
	3	PC_EN	0 – disable phase-cal processing 1 – enable phase-cal processing
	2	ERF	Error was found by TVR on selected bit streams(s) – [read only]
	1	CHECK	TVR checking has started – [read only]
	0	GOCOM	Start checking VSI input for TVG sequence on next selected 1pps.
2	15-0		Spare
3	15-0	IVP_WORD_L	LSB's of 'invalid' data pattern to be output when FPDP word contains any data bit which has been marked invalid by PVALID=0 (when PVALID is enabled with PVENBL=1)
4	15-0	IVP_WORD_H	MSB's of 'invalid' data pattern
5	15-0	BSM_WORD_L	LSB's of input bit-stream mask; # of active bit-streams must be power of two.
6	15-0	BSM_WORD_H	MSB's of input bit-stream mask
7	15-0	USER_WORD	User-specified field to be copied into Word 1 of each Disk Frame Header
8	15-0	START_TIME_L	16 LSB's of scan BCD start time: ' <u>JJJSSSSS</u> ' (underlined)
9	15-0	START_TIME_H	16 MSB's of scan BCD start time: ' <u>JJJSSSSS</u> ' (underlined)
A	10	CGW_CLK	Clock Generator write clock (set and cleared to simulate a clock)
	9	CGRESET	'1' resets Clock Generator
	8	CGFQ_UD	Transition 0→1 sets CG to updated value
	7-0	CG	Clock Generator configuration byte (5 successive bytes needed to set CG)
B	15	RESET_PPS	1 – reset PPS-counter and SUNKPPS flag 0 - PPS-counter is operating (but not necessarily sync'ed)
	8	CLRPPSFLAGS	Clear APERTURE_SYNC and EXACT_SYNC flags; holds them clear as long as value is '1'. '0' causes resumption of checking selected input PPS against DOT1PPS.
	7	INVALIDATE	1 - forces data to 'invalid' pattern
	6	PVENBL	1 - use PVALID pin to determine data validity. 0 - ignore PVALID pin. Note: If bits 6 & 7 of word B are both '0', data is never marked invalid.
	5	PAUSE	1 - stops data flow to FPDP bus at next DF boundary; does not stop the Disk Frame header generator. 0 - starts data flow to FPDP bus on next DOT1PPS tick. Note: PAUSE may only be set while START/STOP is '1'; PAUSE may be used to stop and start recording without re-issuing SETUP as long as the recording parameters do not change.
	4	START/STOP	1 – starts data flow to FPDP bus on next DOT1PPS tick; must be issued sometime within second previous to START_TIME. 0 - stops data flow to FPDP bus at next DF boundary; stops DF header generator
	3	Spare	
	2	SYNCPPS	0→1 transition resets SUNKPPS bit, causes DOT1PPS to synchronize to the next

			occurrence of the 1PPS signal selected by SELPP.
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	1	SETUP	0→1 transition stops Disk Frame Header generator (if already running), configures DIM according to current values of J and BSM and primes DFH generator with START_TIME value; must be issued comfortably ahead of target DOT1PPS tick representing START_TIME. Requires START/STOP=1 to start DFH generator.
	0	RESET	1 - Holds all state machines in the DIM, including phase-cal extractor, to reset value; does not affect value of any configuration parameters. 0 - normal operation. Note: On power-up, all R/W parameters are set to zero.
C	15-0	TVR_MASK_L	TVR mask (15:0)
D	15-0	TVR_MASK_H	TVR mask (31:16)

Read only parameters:

Word	Bit(s)	Name	Description
E	13	II	0 – if set to '0' after REQ_II is set to '1', FPDP bus must operate in FPDP mode 1 – indicates that all devices on FPDP bus are able to operate with FPDP-II protocol
	12	OF	Set to '1' if FIFO overflow detected between S/S=1 and S/S=0 (i.e. start and stop of a scan)
	11	APERTURE_SYNC	Set to '1' if selected 1PPS signal is displaced more than +/-3 input clock cycles from DOT1PPS; active only after successful DOT1PPS sync.
	10	EXACT_SYNC	Set to '1' if selected 1PPS signal is not coincident with DOT1PPS; active only after successful DOT1PPS.
	9	SUNKPPS	Set to '1' on successful synchronization (initiated by SYNCPPS 0→1 transition); cleared by SYNCPPS 0→1 transition.
	8	F_OK_FLAG	Set to '1' during SETUP if number of 1's in BSM field is power of two.
	7-0	REV_BYTE	Current DIM revision level
F	15-0	HDR_WORD_2_L	LSB's of Word 2 of last-generated Disk Frame Header; the header words 2 & 3 are placed in this area at the time they are created. After SETUP is issued, the value is static until header generation is started with Start/Stop=1 and remains dynamic until another SETUP or RESET is issued. When dynamic, the generation of the headers will lag real-time by 2 to 6 msec at 2 Mbps aggregate data rate and 4 to 12 usec at 1024 Mbps aggregate data rate.
10	15-0	HDR_WORD_2_H	MSB's of Word 2 of last-generated Disk Frame Header.
11	15-0	HDR_WORD_3_L	LSB's of Word 3 of last-generated Disk Frame Header.
12	15-0	HDR_WORD_3_H	MSB's of Word 3 of last-generated Disk Frame Header.
13	13	DOT1PPSINT_ERR	Set to '1' if a second DOT1PPSINT interrupt occurs before the prior one is cleared
	12	DOT1PPSINT	DOT1PPS interrupt, latched; reading the register clears this bit.
	11	DIM1PPSINT	DIM external 1PPS interrupt, latched; reading the register clears this bit.
	10	DIM1PPSINT_ERR	Set to '1' if a second DIM1PPSINT interrupt occurs before the prior one is cleared
	9	PC_INT_ERR	Set to '1' if a second phase-cal interrupt occurs before the prior one is cleared
	8	PC_INT	Phase-cal interrupt (latched); reading the register clears this bit

Typical sequence of operations

The following is a typical sequence of operations from power-up to normal observing:

1. Issue RESET to reset all state machines in DIM (does not affect any settable DIM parameters). Release RESET.
2. Start DOT1PPS generator –
 - a. Set values of TVGSEL, SELTVCNT, K, SELPP and SELCGCLK as required
 - b. Set SYNCPPS=1 to synchronize DOT1PPS tick with external 1PPS tick; SUNKPPS will transition to ‘1’ on successful synchronization.
 - c. Assert, then clear, the CLRPPSFLGS bit to clear APERTURE_SYNC and EXACT_SYNC flags, then monitor every few seconds to check synchronization of DOT1PPS.
3. Start scan –
 - a. Set values of J, BSM_WORD and START_TIME for first scan.
 - b. Issue SETUP (0→1 transition) to prime Disk Frame Header generator. (Must wait >135 data-clock cycles before proceeding to step c)
 - c. Set START/STOP=1 sometime in the DOT second preceding the specified START_TIME to start data flow to FPD bus on next DOT1PPS tick (which will correspond to START_TIME).
 - d. Set START/STOP=0 to stop data flow to FPD bus at end of next Disk Frame.
4. As long as values of J and BSM_WORD do not change, PAUSE may be used to start and stop scans without re-issuing SETUP; otherwise, must re-issue SETUP.

Operation of DIM interrupts

Introduction

The DIM interrupt system consists of three parts. The first part is the mask register, which enables and disables the ability of the interrupt sources to set the interrupt latches. The second part is the interrupt signals themselves. The interrupt latches are the third part and they “remember” the occurrence of an interrupt event. If any latch is set (thus remembering an interrupt event) the PLX chip will cause a PCI interrupt (INTA#).

The mask bits are in word “0” bit 12 (SEL_DOT_1PPS) and bit 11 (SEL_DIM_1PPS). When the bit is a “1” the interrupt is enabled. The mask bits can be set and cleared by the software.

If SEL_DOT_1PPS is a “1” the next occurrence of the internal 1PPs signal will set the DOT1PPSINT latch and cause a PCI interrupt. One of three input signals to the DIM can be selected to be the second interrupt signal. (These are VSI_1PPS, ALTA1PPS, and ALTB1PPS, which are selected by word “0” bits 2 and 1.) If SEL_DIM_1PPS is a “1”, the next occurrence of the second interrupt signal will set the latch DIM1PPSINT, thus causing a PCI interrupt.

The software can read the status of the interrupt latches by reading word 13 (hex) bit 12 for DOT1PPSINT and bit 11 for DIM1PPSINT. The result of reading word 13 is to reset bits 11 and 12. These bits can only be set by the enabled interrupt signals.

Initialization

In order to initialize the interrupt system it is necessary to clear the interrupt latches of any spurious values by disabling both interrupts and reading word 13 (hex). Then clear any PCI interrupt, which may be due to the spurious values.

Operation

It is expected that only one interrupt will be enabled at any one time. It is also expected that, with the exception of the initialization, word 13 (hex) be only read in response to a PCI interrupt event.

Error Detection

Each interrupt has an associated error bit. The error bit will become '1' if a second interrupt event occurs before the associated interrupt latch is cleared. The idea is that each interrupt should be answered before it can occur again. The error bit DOT1PPSINT_ERR is located in word 0x13 bit 13. The error bit DIM1PPSINT_ERR is located in word 0x13 bit 10. The error bits are cleared (set to '0') after location 0x13 is read.

Operation of the DIM TVR

The DIM contains a test vector receiver (TVR) which can be used to check incoming data streams for errors when the stream is the standard test vector sequence as defined in the VSI-H specification.

A few precautions apply. The selected input clock must be the VSI input clock, not the internal clock generator. (Set the parameter SELCGCLK to "0". This is bit 0 of word 0 in the DIM parameter field.) Also the external 1PPS source must be set to be the VSI1PPS. (Set the parameter SELPP to the value "3" in bits 2 and 1 of word 0 in the DIM parameter field.)

The operation of the DIM TVR is controlled by the parameter GOCOM (bit 0 word 1) and the test vector mask TVM(31:0) (words 0xC and 0xD). The result of the TVR operation is detected by observing parameters CHECK and ERF which are bits 1 and 2 of word 1 respectively.

When GOCOM is set to "1" the TVR control will wait for the next VSI1PPS to start the check for errors. The parameter CHECK can be read to verify that the TVR has begun checking. Once checking has started each bit stream selected by having a "1" in its test vector mask is compared with the expected value for that bit stream. If any selected bit stream is found in error, the parameter ERF will be set to "1". Checking continues until GOCOM is set to "0", at which point the TVR stops checking and sets CHECK to "0" when it finds the next occurrence of VSI1PPS. It is assumed that the parameter GOCOM changes state away from the occurrence of VSI1PPS transitioning from "0" to "1".

ERF is cleared when checking begins or by the assertion of a DIM reset (bit 0 of parameter word 0xB). The interpretation of ERF is that one or more errors was detected. LED #5 is red whenever ERF is a "1". LED #5 is green when CHECK is "1" and ERF is "0" (i.e. TVR is active with no detected errors).

Operation at 2 Gb/s

The DIM can be set to receive data at 2048 Mbps and record it on disks via the FPDP bus. In order to do this several parameter settings are required.

A data rate of 2048 Mbps implies that there are 32 input streams being clocked at 64 MHz. Thus the parameter “K” must be set to a value of 5. The internal clock generator cannot be set to the value of 64 MHz so the clock must be input from the VSI connection. This implies that “SELGCLOCK” (Word 0 bit 0) must be set to the value “0”.

The FPDP interface on the Mark 5B board can only write the 2GB/s data if the FPDP bus is set to operate in the FPDP II mode. The following steps accomplish this:

1. Request FPDP II by setting REQ_II (word 0 bit 13) to “1”.
2. Read the parameter II (word E bit 13).
 - a. II = 1 implies that the bus is capable and the DIM will operate in FPDP II mode.
 - b. II = 0 implies that the bus will not run in FPDP II mode. Set REQ_II back to “0”.