Correlator implementation and control meeting

October 4 and 6 2011, Arpad's room

present Jonathan, Salvatore, Harro, Des, Arpad

Question of what format input data should have. VDIF frames (Mark5C format), 1 or 2 pols per packet. For the time being only 1 pol. Program needed to send number of UDP packets over 10G. 4 subbands, one containing sine wave, the other zeroes. Des has something on shelf, will make the program. Before end of week (...?)

What output format. As described in correlator doc on wiki, should be adequate. For the time being, data will be output over 1 G, via NIOS, for inspection. Next step via 10 G. How to distribute data over available ports to be decided later on, might be easiest to leave ordering of output data to offline system.

Delay model/rot clock. Not quite clear if rot clock is needed at all. It is possible to determine length of processing time by inspecting output data, adjust input rate.

Second meeting:

lengthy discussion about timing mechanism for recorded playback and real time. Jonathan thinks it will be possible to have FPGAs check fullness of buffers and stop processing of all of them if one of them runs behind. Like this can run at maximum possible speed. Still have output data time code check to fine tune playback speed. In real-time case, uniboard will always run at least at same speed or faster than input rate, may have to pause at times when buffer empties. Des will implement feedback loop, Jonathan will check communication method between FN FPGAs.